

HM42-CP Block Diagram

PCB P/N : 48.4GW01.011
REVISION : -1 09920

Project code: 91.4GW01.001 (HM42-CP)
91.4GY01.001 (JE40-CP)
91.4GZ01.001 (SJV41-CP)
91.4JD01.001 (BA40-CP)

Clock Generator
ICS9LRS3197AKLFT

X2
14.318Mhz

DDRIII Slot 0
800/1066

DDRIII Slot 1
800/1066

20

21

DDRII Channel A

DDR II Channel B

Intel CPU
Arrandale

4, 5, ..., 9, 10

FDI x8

DMI x4

X3
27Mhz

N11P-GE1
N11M-GE1
Nvida

RGB CRT

LVDS 1CH

HDMI

CRT

LCD
WXGA+

HDMI

SYSTEM DC/DC
RT8223

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC
RT8209E

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC
RT8209E

INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 1D05V_S0

SYSTEM DC/DC
RT9025

INPUTS	OUTPUTS
DCBATOUT	1D8V_S0

SYSTEM DC/DC
RT8209E

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

SYSTEM DC/DC
TPS5161

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

CPU DC/DC
ISL62882C

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

CHARGER
ISL88731C

INPUTS	OUTPUTS
DCBATOUT	BT+

Discrete N11M

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Block Diagram

Size
A3

Document Number

HM42-CP

Rev

SC

Date: Friday, January 22, 2010

Sheet 1 of 72

Mini-Card
WLAN

Mini-Card
3G

PCIE

USB 2.0

RJ45
CONN

Giga LAN
BCM57780

PCIE

X1
25Mhz

X5
25Mhz

MIC IN

INT MIC

HD AUDIO
CODEC
ALC272

AZALIA

PCB STACKUP

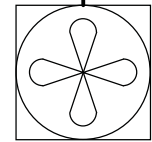
TOP
GND
S
S
GND
BOTTOM

LINE OUT

2CH SPEAKER

OP AMP
G1454

34



CPU FAN

INTEL
PCH
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
6 SATA ports
8 PCIE ports
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE

11, 12, ..., 18, 19

X6
32.768Khz

LPC Bus

LPC debug

X4
32.768Khz

KBC
ENE 3930

SPI

Flash ROM
128KB

Thermal
Sensor

Touch
PAD

Int.
KB

Card Reader
AU 6433

37

SD/MMC
MS/MS Pro/xD

37

SATA HDD

26

SATA ODD

27

Flash ROM
4MB

41

BA40_Power_BD
09768-1

PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

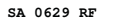
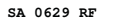
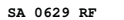
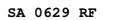
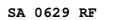
Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1 (HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

Processor Strapping

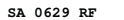
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

<Variant Name>

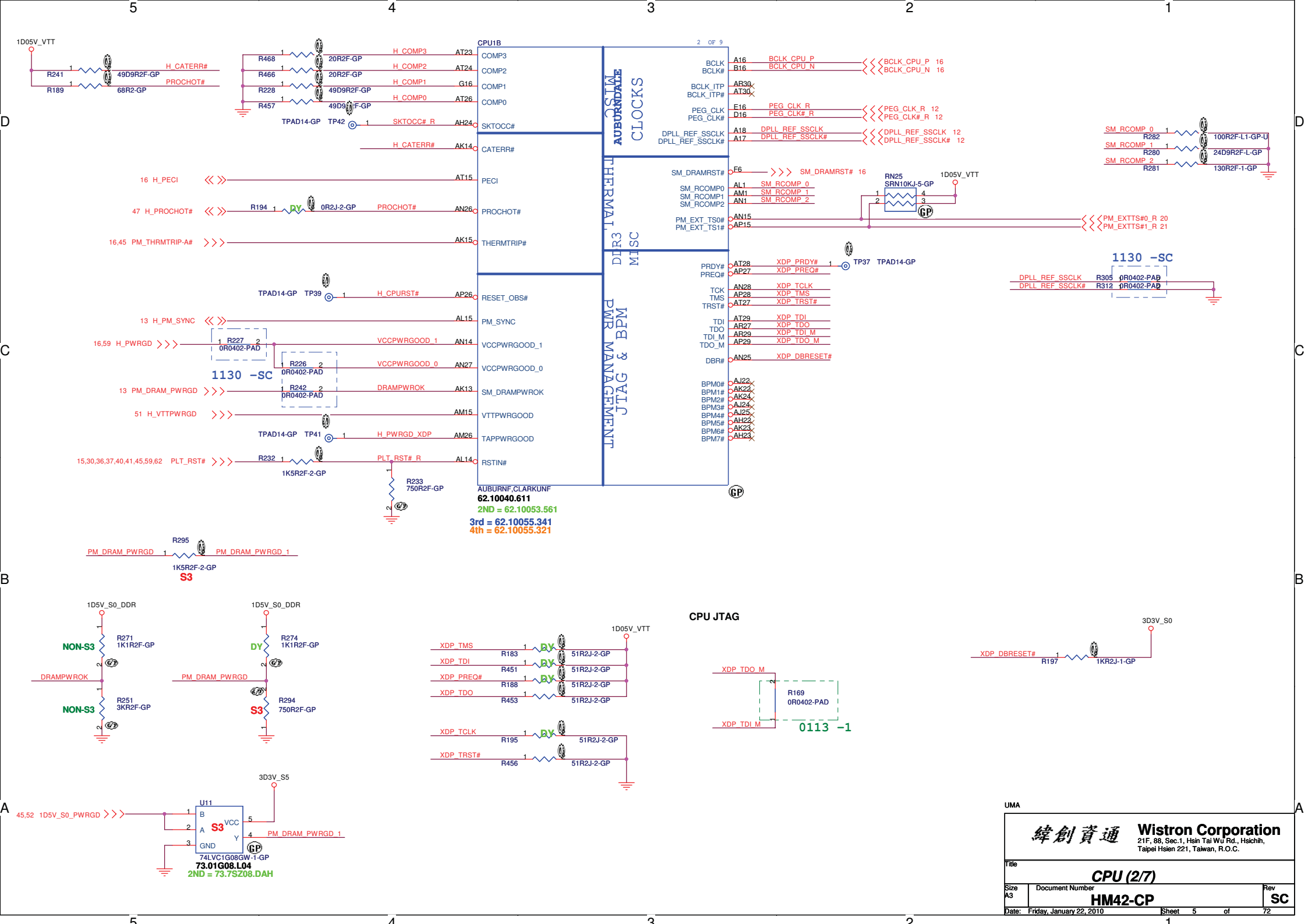
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Table of Content			
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SA 0629 RF



SA 0629 RF



AUBURN CLARKUNF
62.10040.611
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10055.321

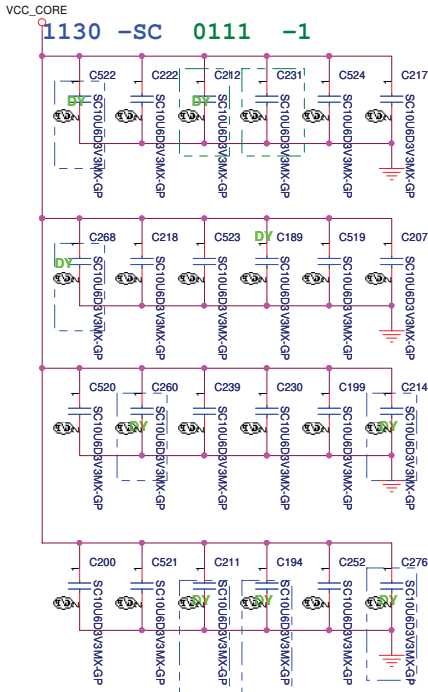


AUBURN CLARKUNF
62.10040.611
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10055.321

<Variant Name> GP

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Title				
CPU (3/7)				
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PROCESSOR CORE POWER

48A

VCC_CORE

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- V35 VCC
- V34 VCC
- V33 VCC
- V32 VCC
- V31 VCC
- V30 VCC
- V29 VCC
- V28 VCC
- V27 VCC
- V26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
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- P28 VCC
- P27 VCC
- P26 VCC

AUBURNDALE

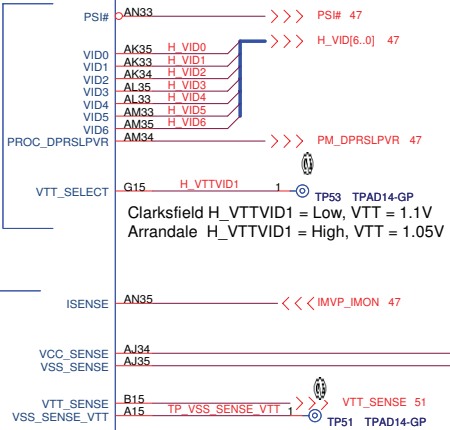
1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES



AUBURNF, CLARKUNF
62.10040.611
2ND = 62.10053.561 3rd = 62.10055.341 4th = 62.10055.321

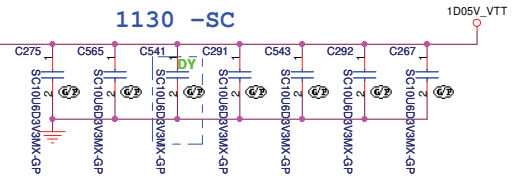


- VTT0 AH14
- VTT0 AH12
- VTT0 AH11
- VTT0 AH10
- VTT0 J14
- VTT0 J13
- VTT0 H14
- VTT0 H12
- VTT0 G14
- VTT0 G13
- VTT0 G12
- VTT0 F14
- VTT0 F13
- VTT0 F12
- VTT0 E11
- VTT0 E14
- VTT0 E12
- VTT0 D14
- VTT0 D12
- VTT0 D11
- VTT0 C14
- VTT0 C13
- VTT0 C12
- VTT0 C11
- VTT0 B14
- VTT0 B12
- VTT0 A14
- VTT0 A13
- VTT0 A12
- VTT0 A11

- VTT0 AF10
- VTT0 AE10
- VTT0 AC10
- VTT0 AB10
- VTT0 Y10
- VTT0 W10
- VTT0 U10
- VTT0 T10
- VTT0 J12
- VTT0 J11
- VTT0 J16
- VTT0 J15

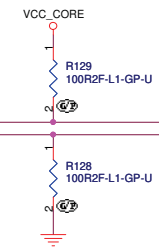
1130 -SC

1130 -SC



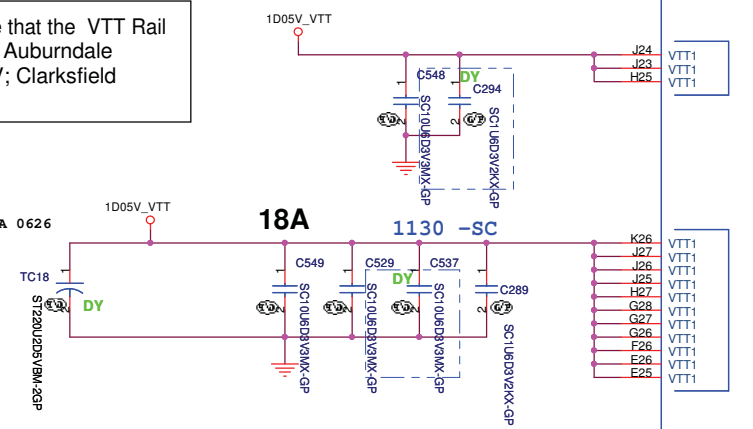
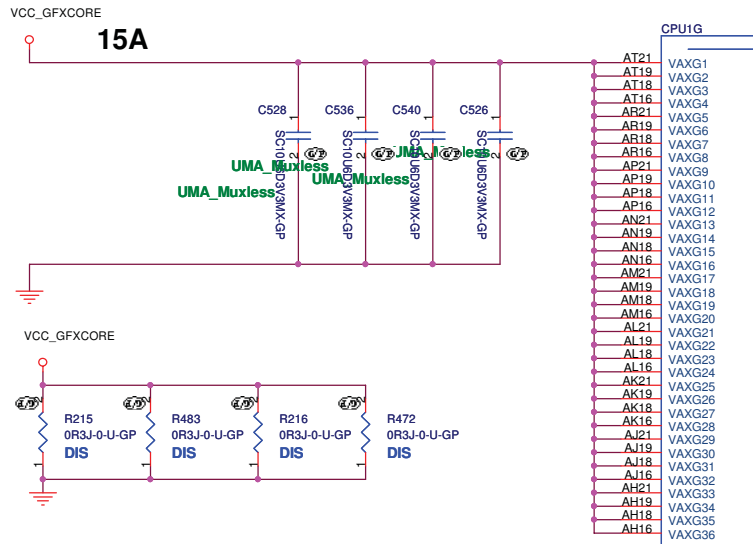
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale
VTT=1.05V; Clarkfield
VTT=1.1V



<Variant Name>

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Title CPU (4/7)			
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Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

POWER

AUBURNDALE

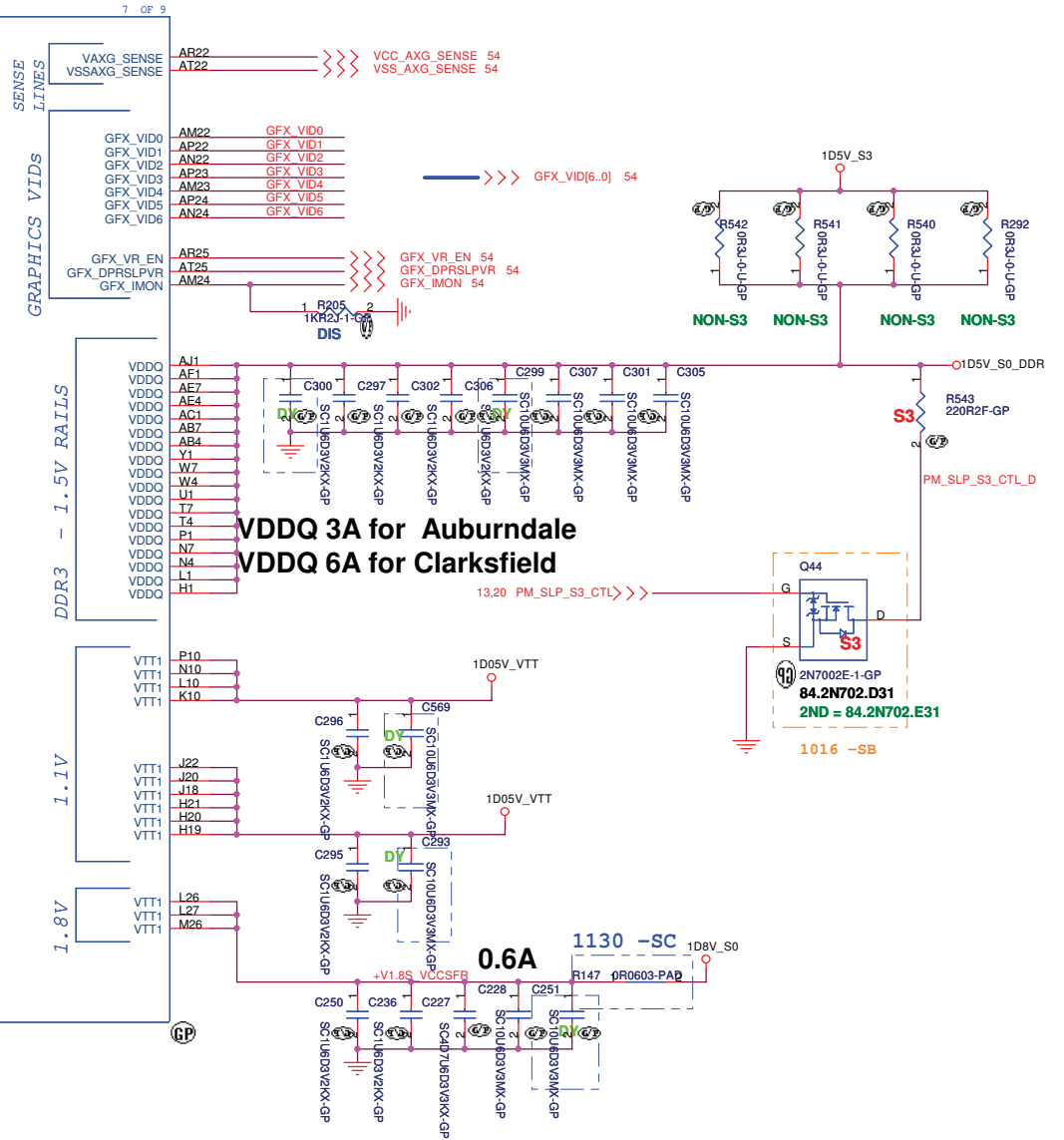
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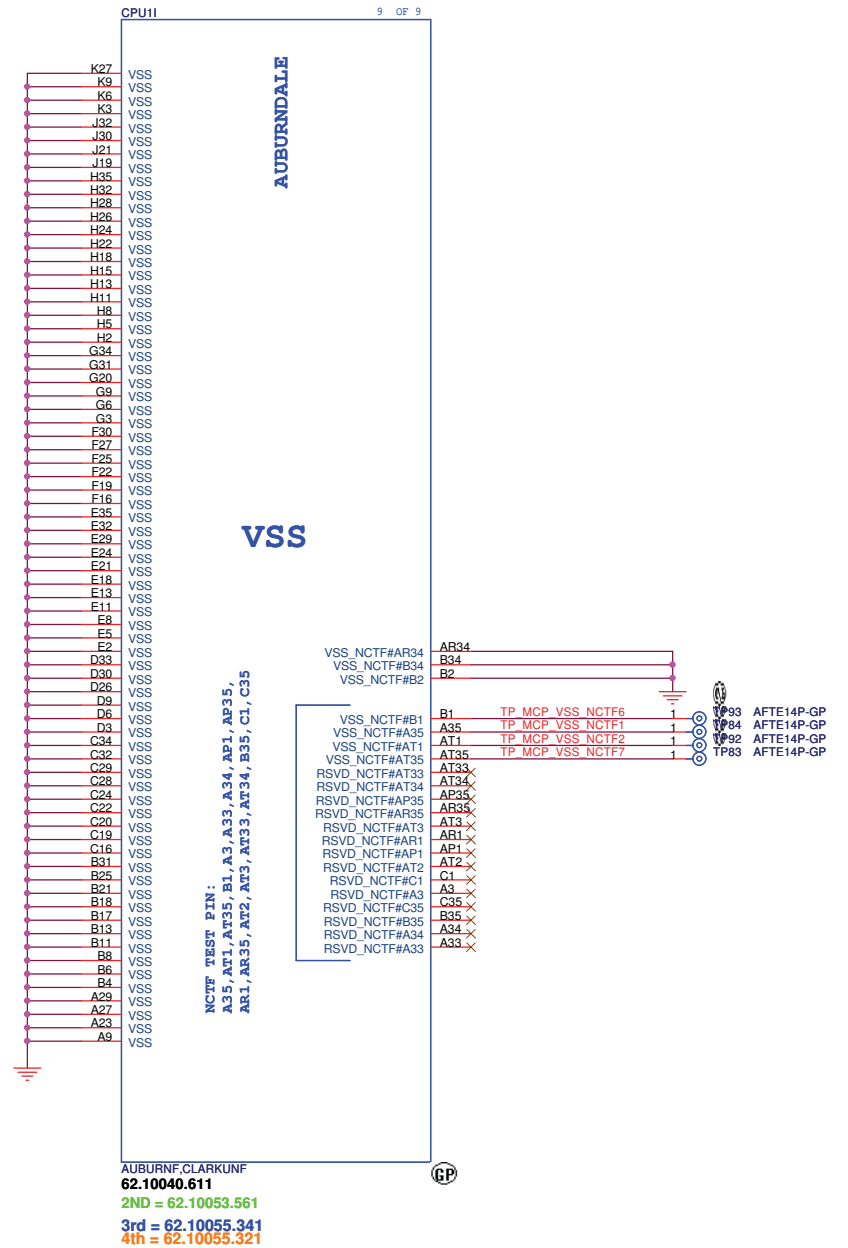
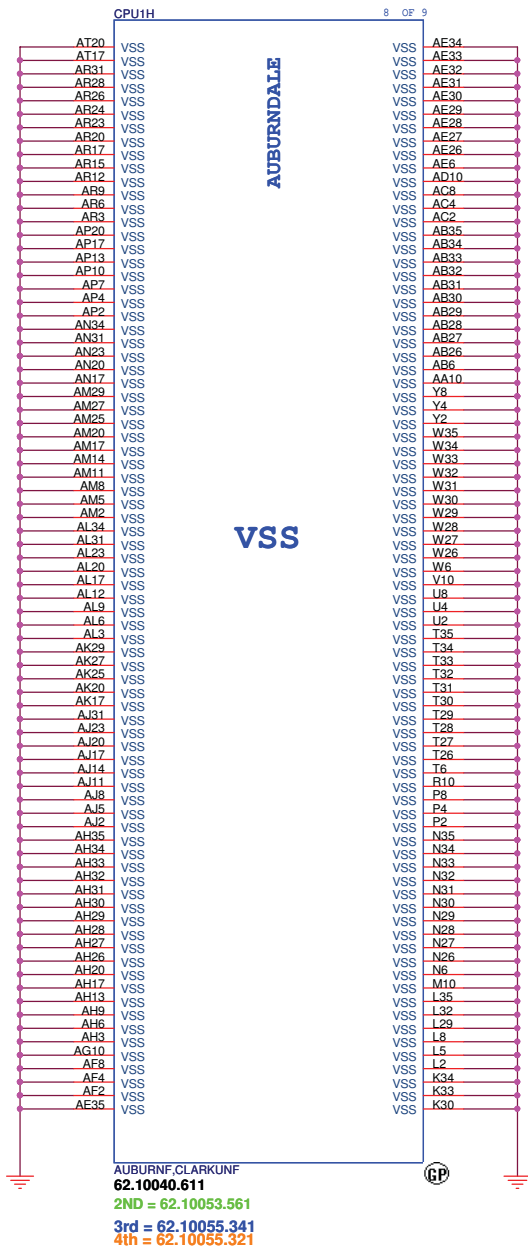
DDR3 - 1.5V RAILS

1.1V

1.8V

PEG & DMI

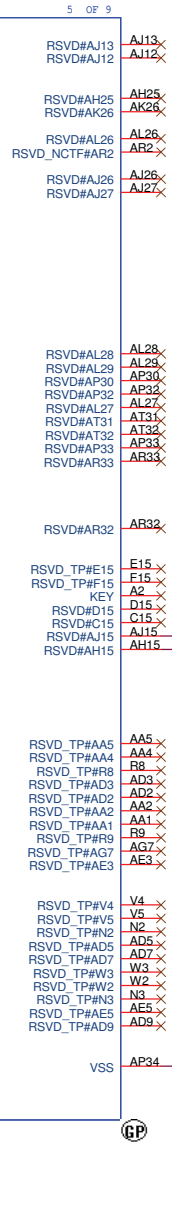
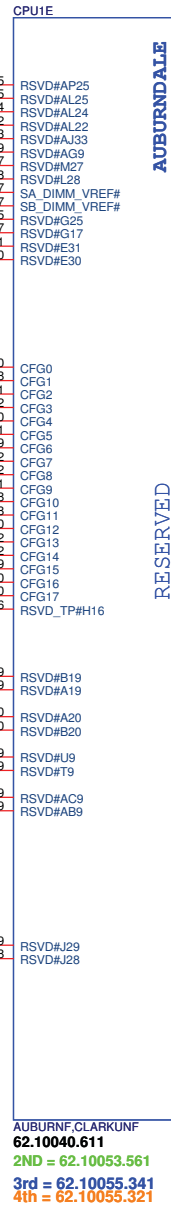
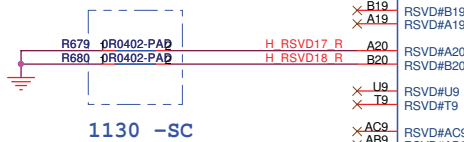
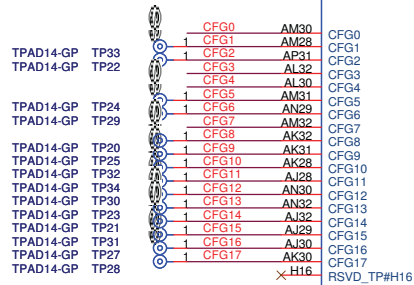
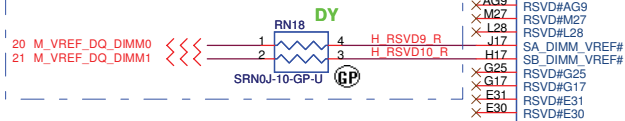




<Variant Name>

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CPU (6/7)		
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SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor



1130 -SC

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



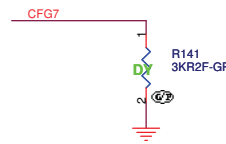
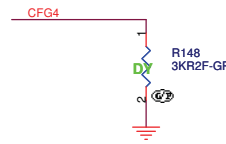
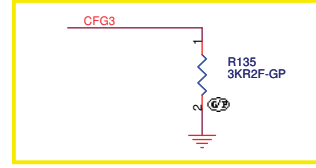
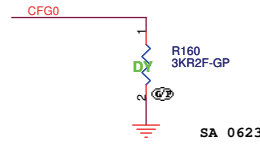
Processor Strapping

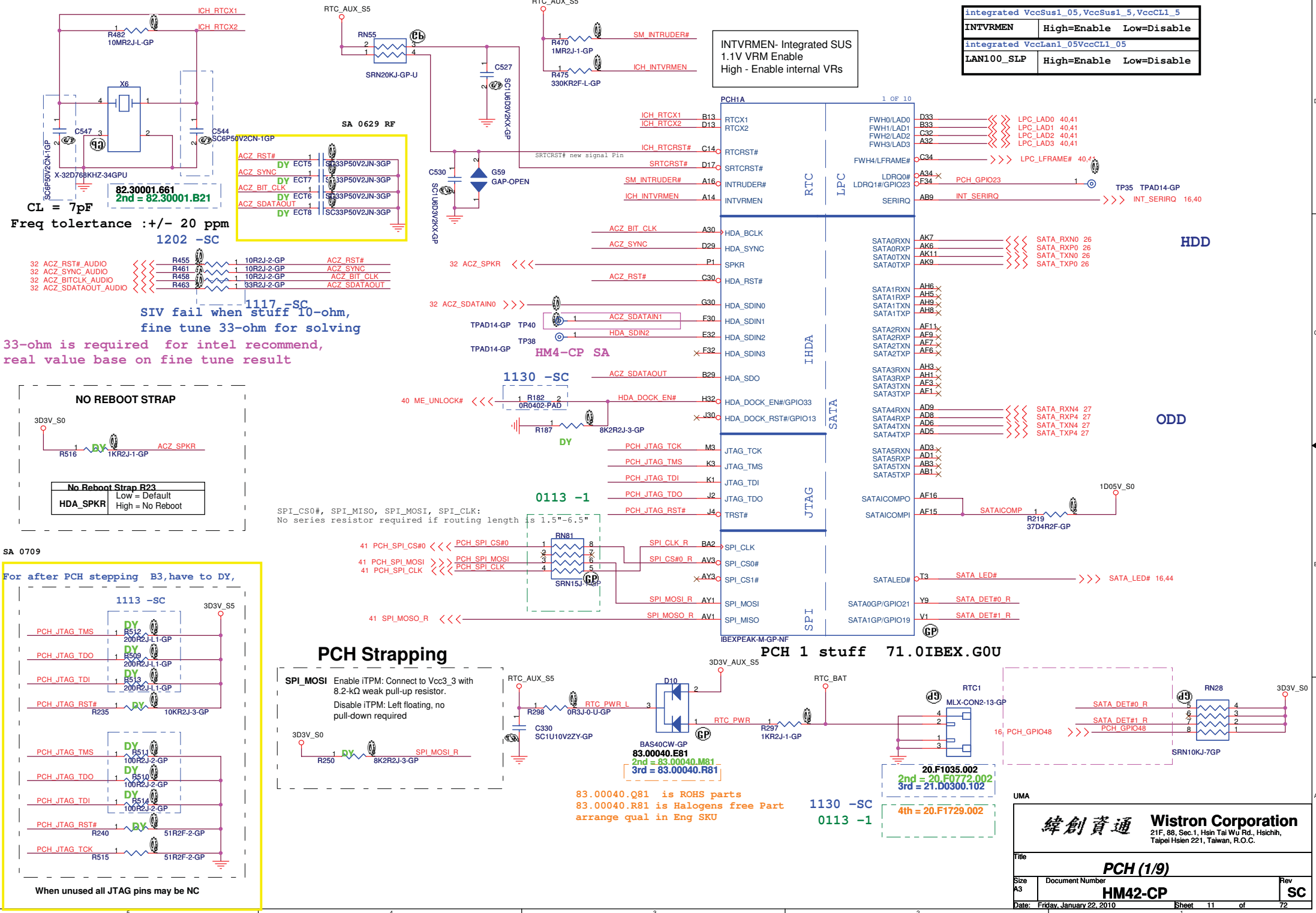
PCI-Express Configuration Select	
CFG0	1:Single PEG(Default) 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation(Default) 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (Default) 0:Enabled; An external Display Port device is connected to the Embedded Display Port

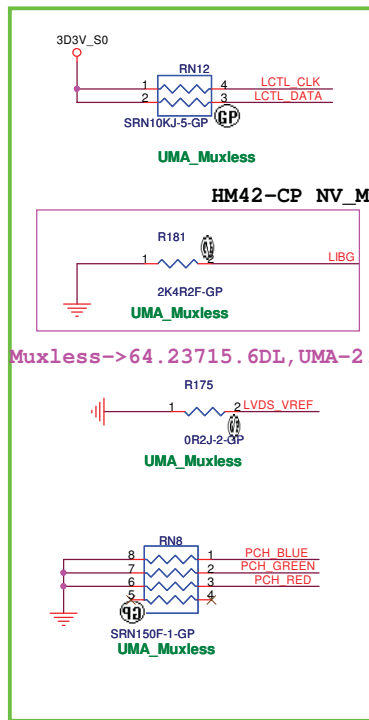
CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.



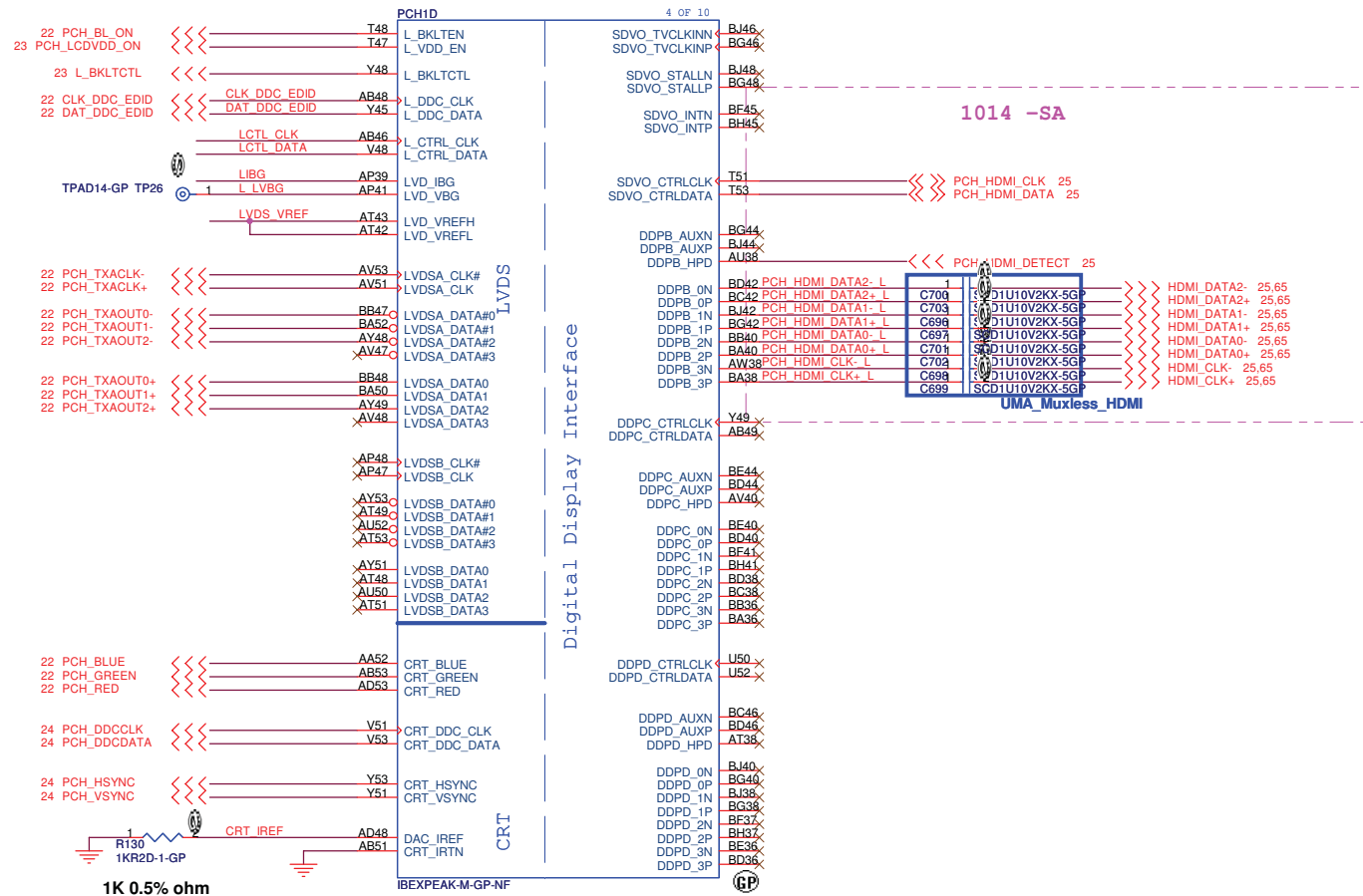








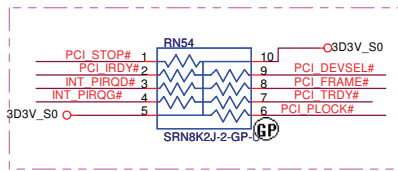
SB 0811



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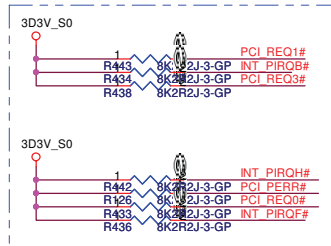
緯創資通 Wistron Corporation
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Taipei Hsin 221, Taiwan, R.O.C.

Title			PCH (4/9)	
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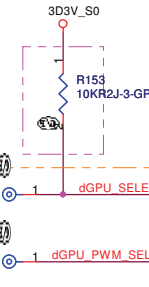


HM42 NV Muxless SA 0925

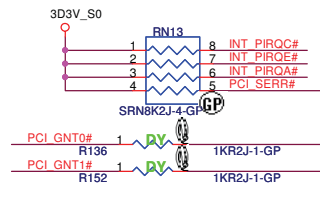
1209 -SC



HM42 NV Muxless SA 0924



1016 -SB

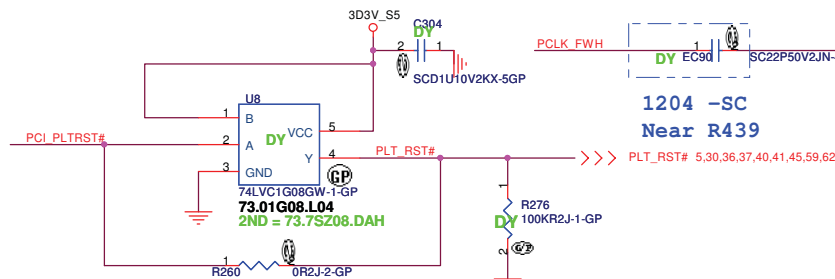


PCH strapping

BOOT BIOS Strap		
GNT#0	GNT#1	BOOT BIOS Location
0	0	LPC
1	0	Reserved
floating	0	PCI
floating	floating	SPI (Default)

PCI_GNT#1	
1	Default (internal pull up)
0	Configures DMI for ESI compatible operation (Not for Mobile platform)

41 PCLK_FWH
42 CLK_PCI_FB
40 CLK_PCI_KBC



1204 -SC
Near R439

PCH strapping

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

These pins are left as NC,
because the function is disable.

These pins are left as NC,
because the function is disable.

PCH strapping

NV_CLE	DMI termination voltage
floating	internal pull-up

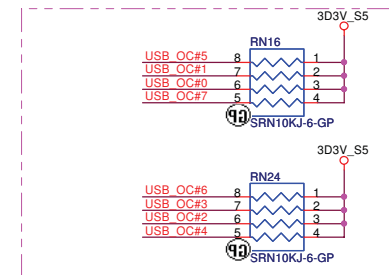
NV_ALE	
1	Enable Anti-Theft Tech
floating	Disable (internal pull down)

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

USB

Pair	Device
0	USB3
1	USB2
2	NC
3	MINICARD1 (WLAN)
4	WECAM
5	NC
6	NC
7	NC
8	3G SIM Card
9	USB1 (HS)
10	NC
11	Blue Tooth
12	MINIC2 (3G)
13	Cardreader

-SA 1001
HM42-CP SA



1006 -SA swap net

<Variant Name>

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GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

HM42-CP_NV_Muxless SA

62 DGPU_HOLD_RST# >>> DGPU_HOLD_RST#
55,61,62 DGPU_PWROK >>> DGPU_PWROK

TPAD14-GP TP36
TPAD14-GP TP46
TPAD14-GP TP45
TPAD14-GP TP56

12 PCH_GPIO11 <<< PCH_GPIO11
EC_SW# <<< EC_SW#
12 PCH_GPIO60 <<< PCH_GPIO60
PCH_GPIO28 <<< PCH_GPIO28

SRN10KJ-7GP
R30
3D3V_S5

PCH_GPIO45 <<< PCH_GPIO45
R508 8K2R2J-3-GP

SB 0819
PCH_GPIO15 <<< PCH_GPIO15
R266 1K2R2J-1-GP

PSW_CLR# <<< PSW_CLR#
GAP-OPEN
G111

11,44 SATA_LED# <<< SATA_LED#
PCH_GPIO39 <<< PCH_GPIO39
INT_SERIRQ <<< INT_SERIRQ
PSW_CLR# <<< PSW_CLR#

SRN10KJ-7GP
RN29
3D3V_S0

STP_PCI# <<< STP_PCI#
PCH_GPIO22 <<< PCH_GPIO22
PCH_GPIO2 <<< PCH_GPIO2
dGPU_EDID <<< dGPU_EDID

3D3V_S0 <<< 3D3V_S0
SRN10KJ-L3-GP

PCH_GPIO35 <<< PCH_GPIO35
10K2R2J-3-GP R265

SB 0722
AFTE14P-GP TP806
AFTE14P-GP TP88
AFTE14P-GP TP87
AFTE14P-GP TP82

1 PCH TP95
1 PCH TP96
1 PCH TP97
1 PCH TP98

SB 0812
3D3V_S5
UMA_Muxless
R239 10K2R2J-3-GP
R238 10K2R2J-3-GP
UMA_DISCRETE#
DIS ONLY: LOW

UMA_Muxless
R239 10K2R2J-3-GP
R238 10K2R2J-3-GP
UMA_DISCRETE#
DIS ONLY: LOW

UMA_Muxless
R239 10K2R2J-3-GP
R238 10K2R2J-3-GP
UMA_DISCRETE#
DIS ONLY: LOW

UMA_Muxless
R239 10K2R2J-3-GP
R238 10K2R2J-3-GP
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DIS ONLY: LOW

UMA_Muxless
R239 10K2R2J-3-GP
R238 10K2R2J-3-GP
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DIS ONLY: LOW

UMA_Muxless
R239 10K2R2J-3-GP
R238 10K2R2J-3-GP
UMA_DISCRETE#
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UMA_Muxless
R239 10K2R2J-3-GP
R238 10K2R2J-3-GP
UMA_DISCRETE#
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UMA_Muxless
R239 10K2R2J-3-GP
R238 10K2R2J-3-GP
UMA_DISCRETE#
DIS ONLY: LOW

UMA_Muxless
R239 10K2R2J-3-GP
R238 10K2R2J-3-GP
UMA_DISCRETE#
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UMA_Muxless
R239 10K2R2J-3-GP
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UMA_DISCRETE#
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UMA_DISCRETE#
DIS ONLY: LOW

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R239 10K2R2J-3-GP
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UMA_DISCRETE#
DIS ONLY: LOW

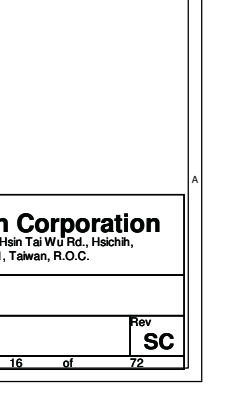
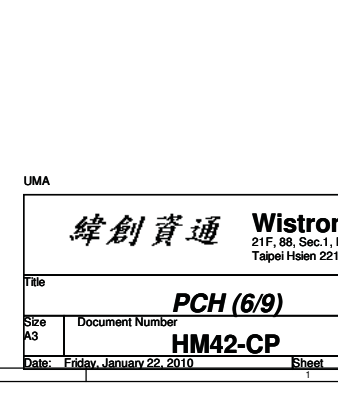
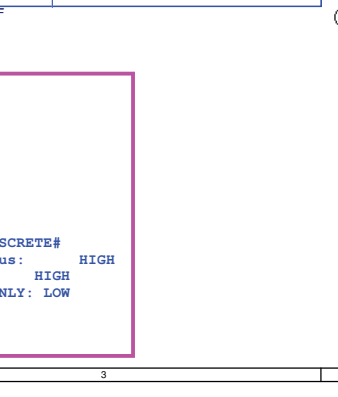
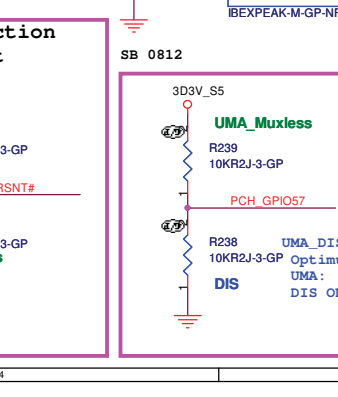
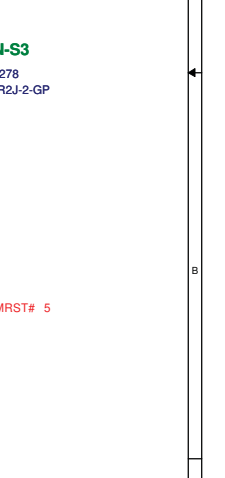
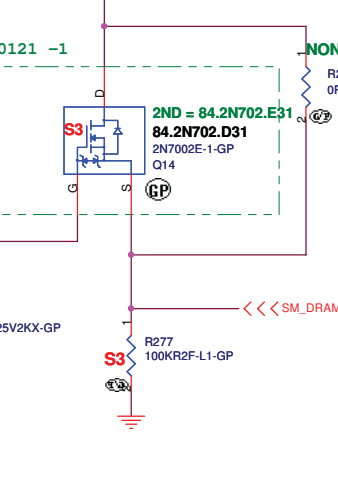
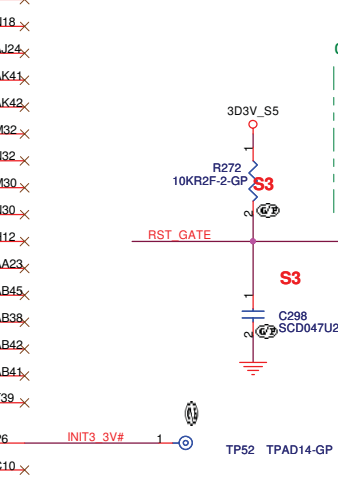
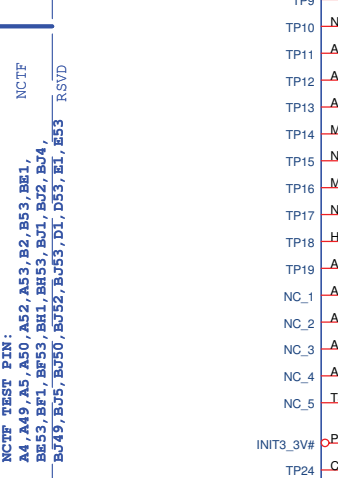
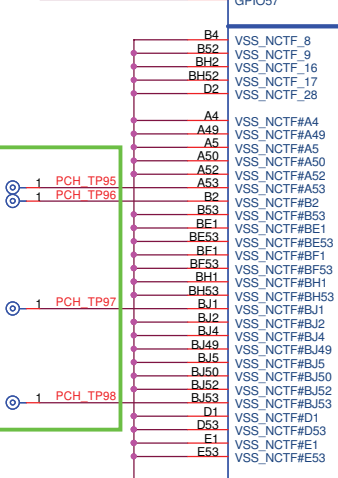
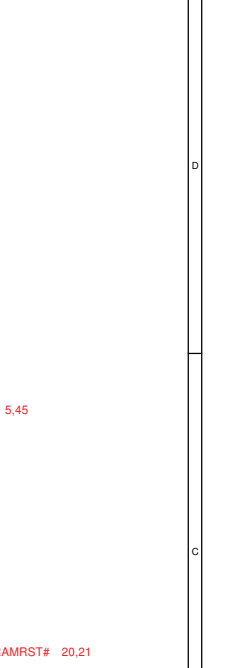
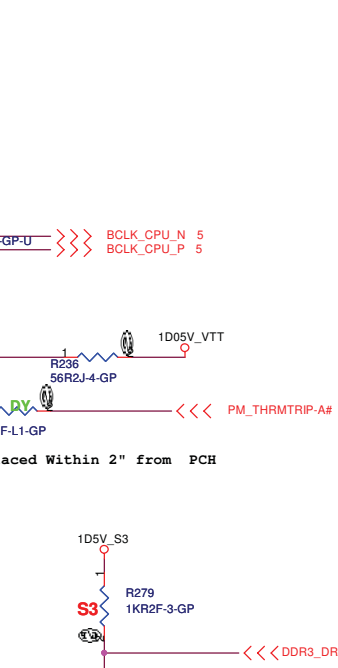
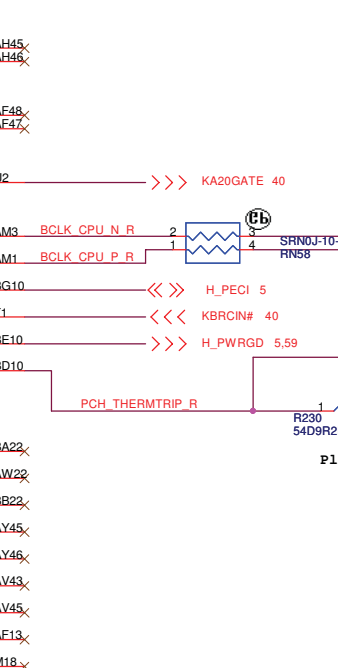
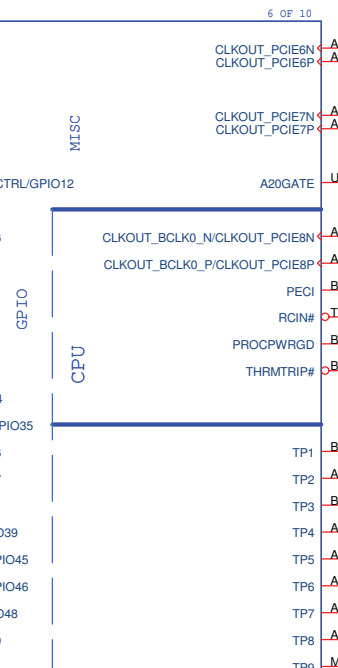
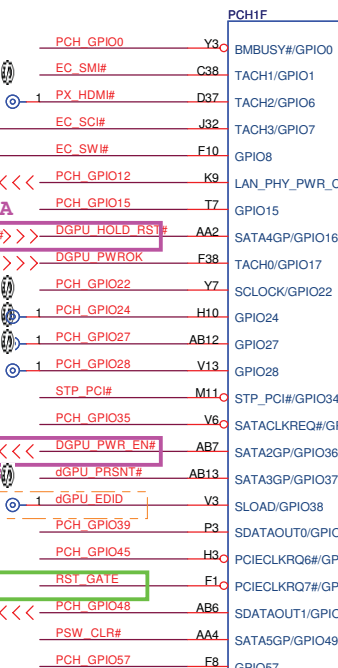
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R239 10K2R2J-3-GP
R238 10K2R2J-3-GP
UMA_DISCRETE#
DIS ONLY: LOW

UMA_Muxless
R239 10K2R2J-3-GP
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UMA_DISCRETE#
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UMA_Muxless
R239 10K2R2J-3-GP
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UMA_DISCRETE#
DIS ONLY: LOW



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Title

PCH (6/9)

Size

A3

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Date

Friday, January 22, 2010

Sheet

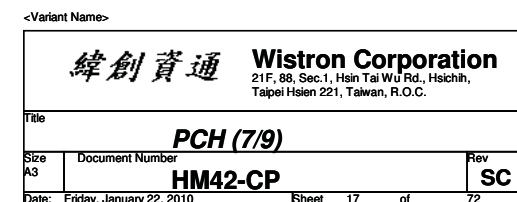
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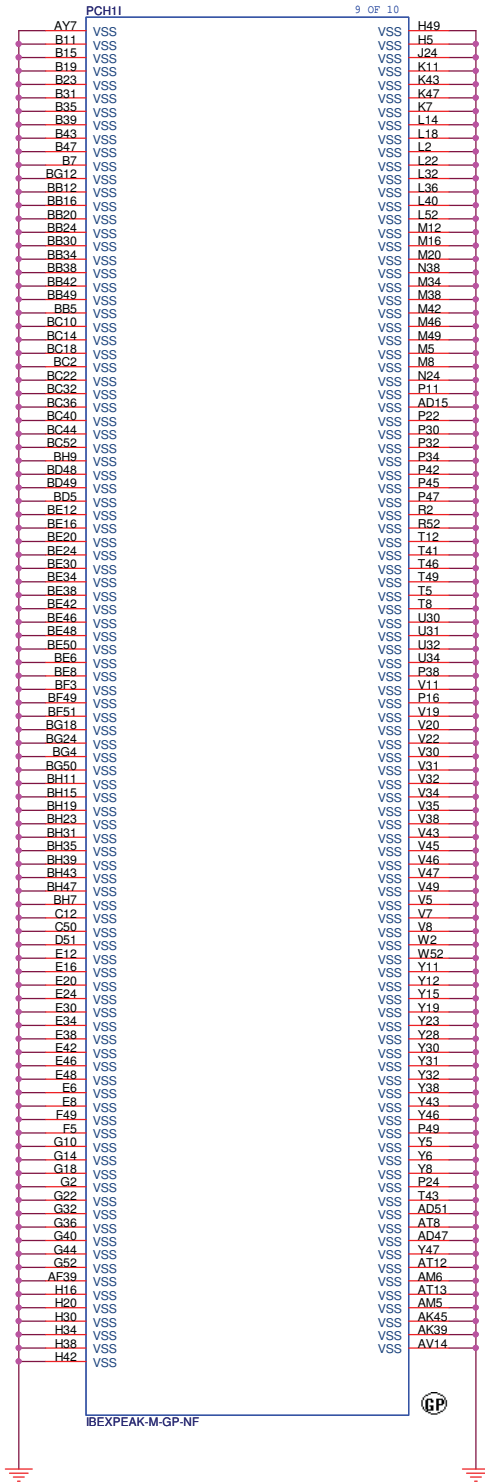
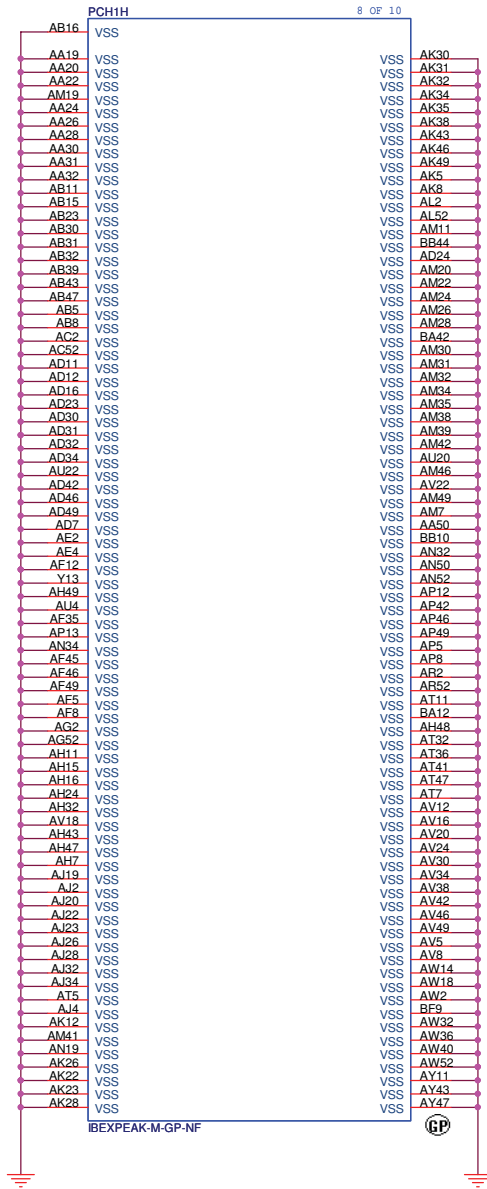
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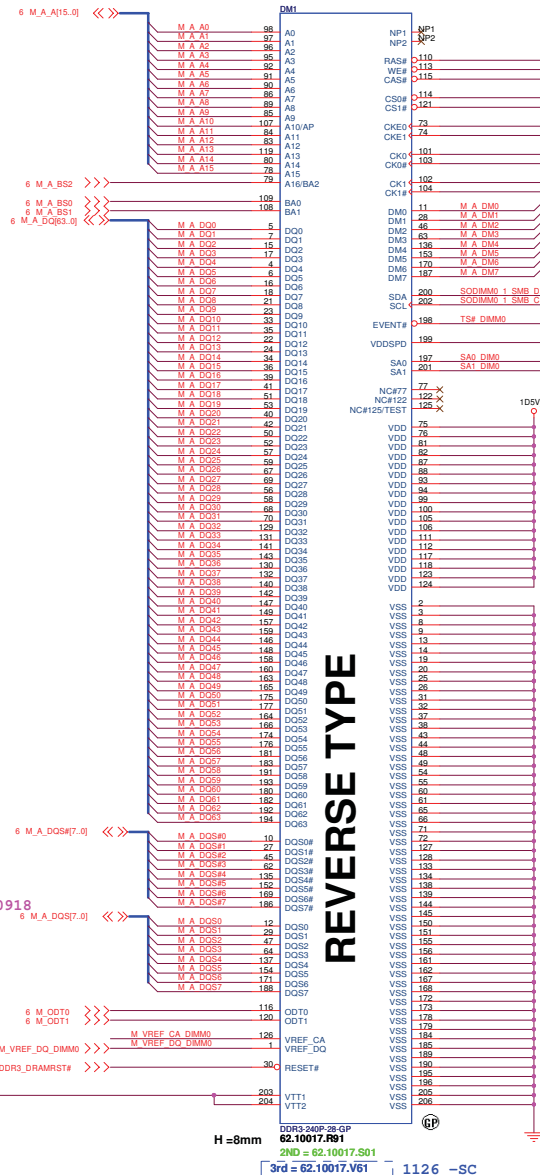
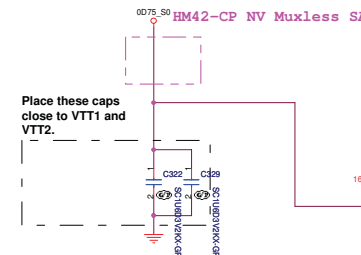
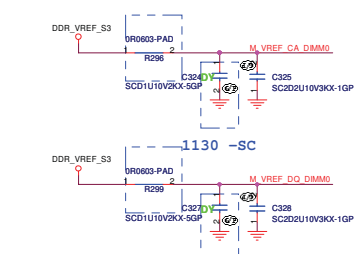
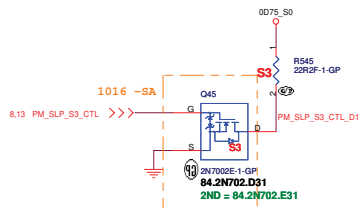
72

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SC

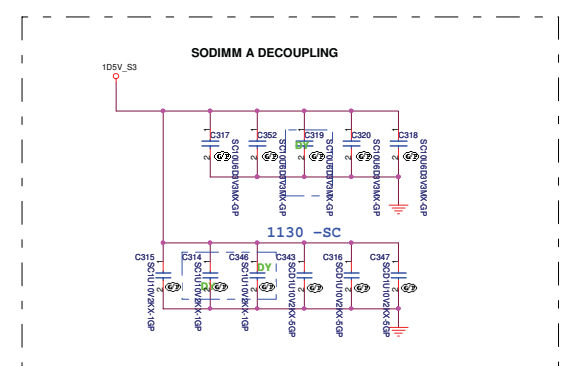
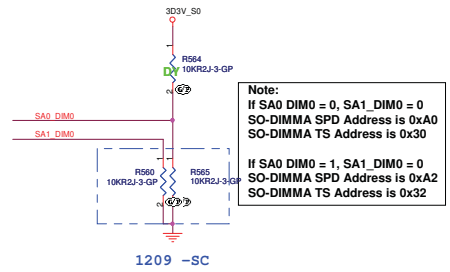






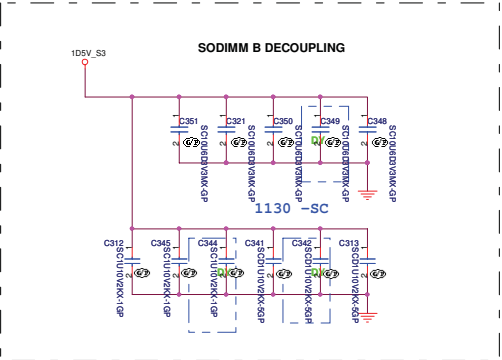
REVERSE TYPE

Layout Note:
Place these Caps near
SO-DIMMA.

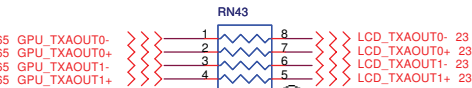
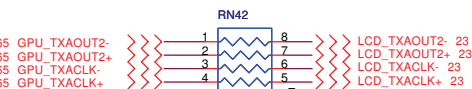
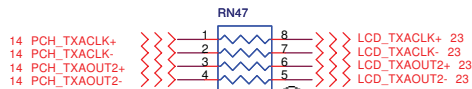
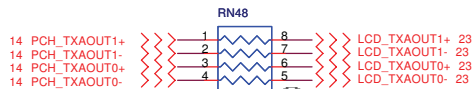


Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

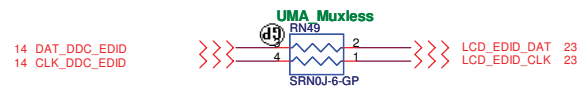
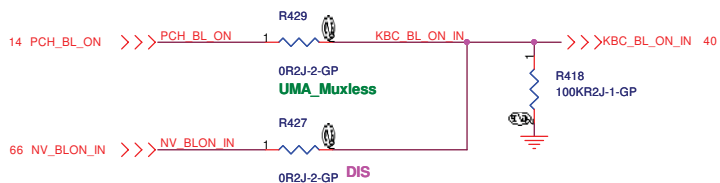
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



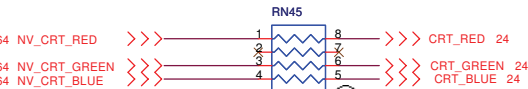
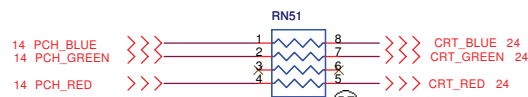
SO-DIMMB is placed farther from the Processor than SO-DIMMA



1016 -SB



1016 -SB



UMA

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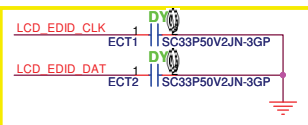
SC

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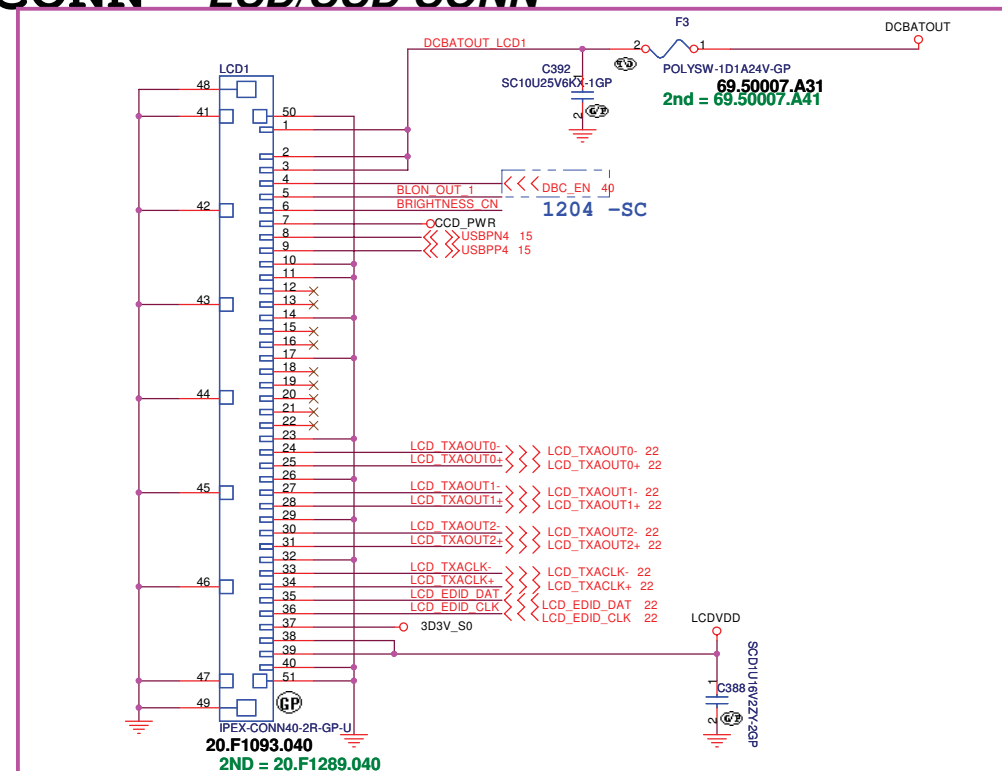
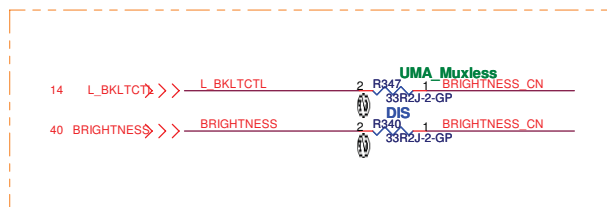
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LCD/INVERTER/CCD CONN

LCD/CCD CONN

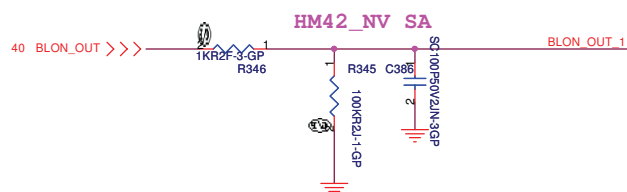


1016 -SB

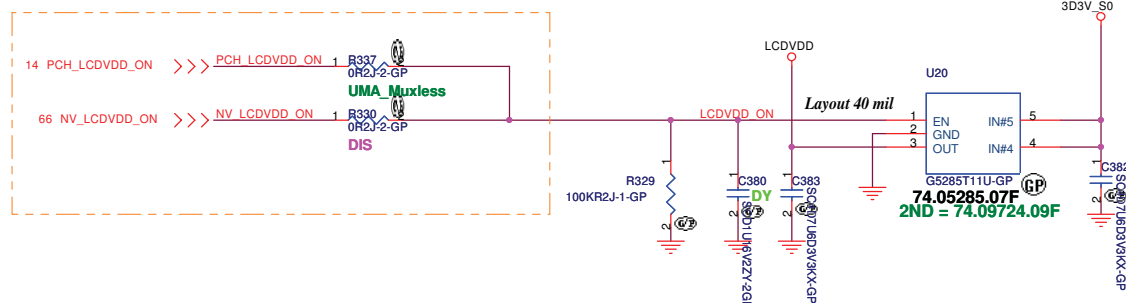


1005 -SA

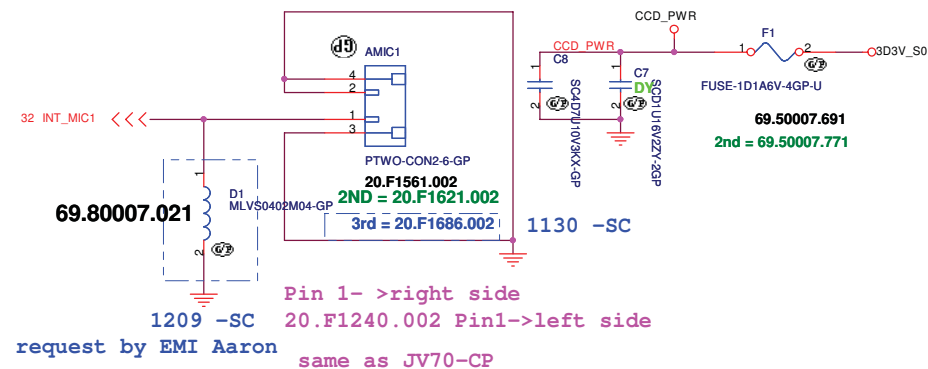
define same as SJM50-PU, can use SJM50 Cable



1016 -SB



Internal Mic



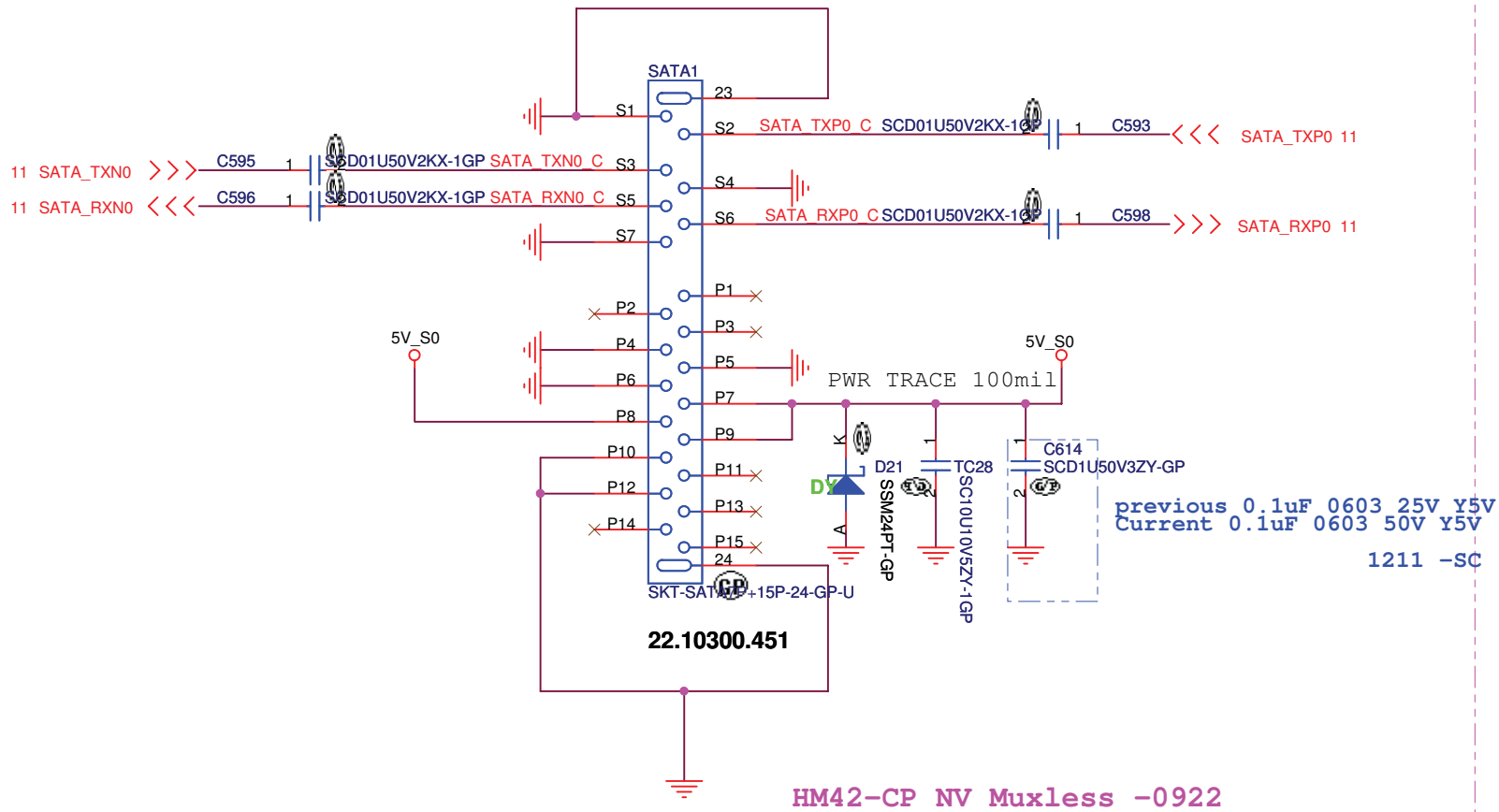
Discrete N11M

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SATA Connector



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Title

HDD CONN

Size

Document Number

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SC

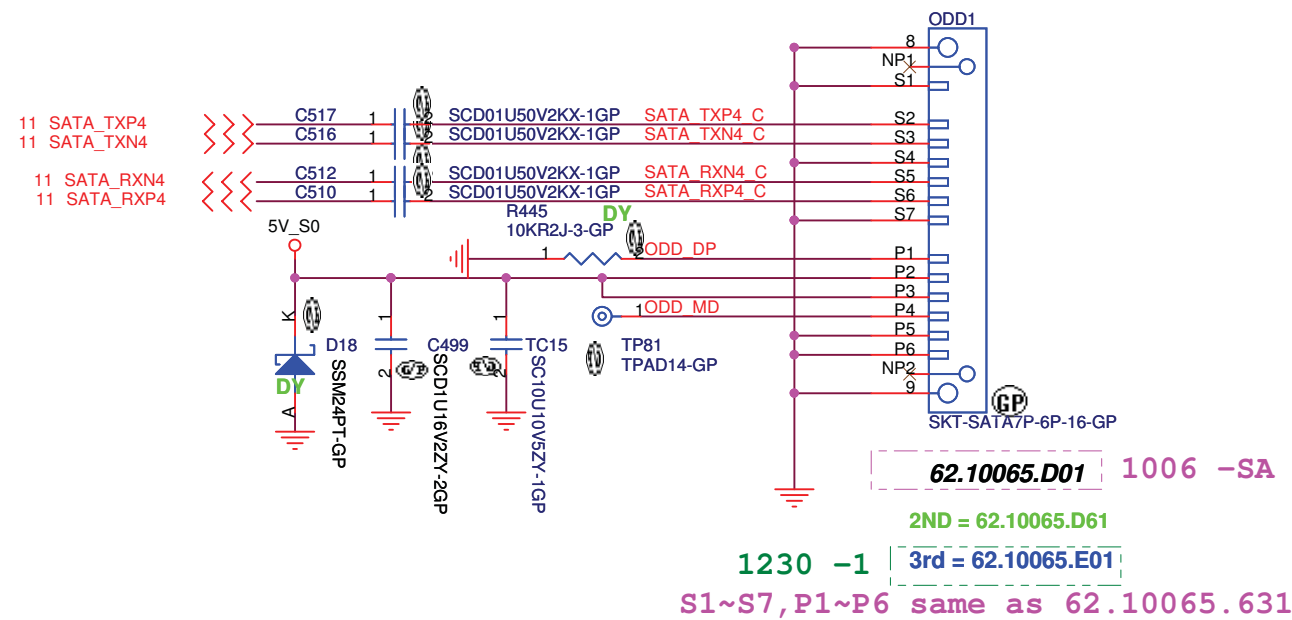
Date: Friday, January 22, 2010

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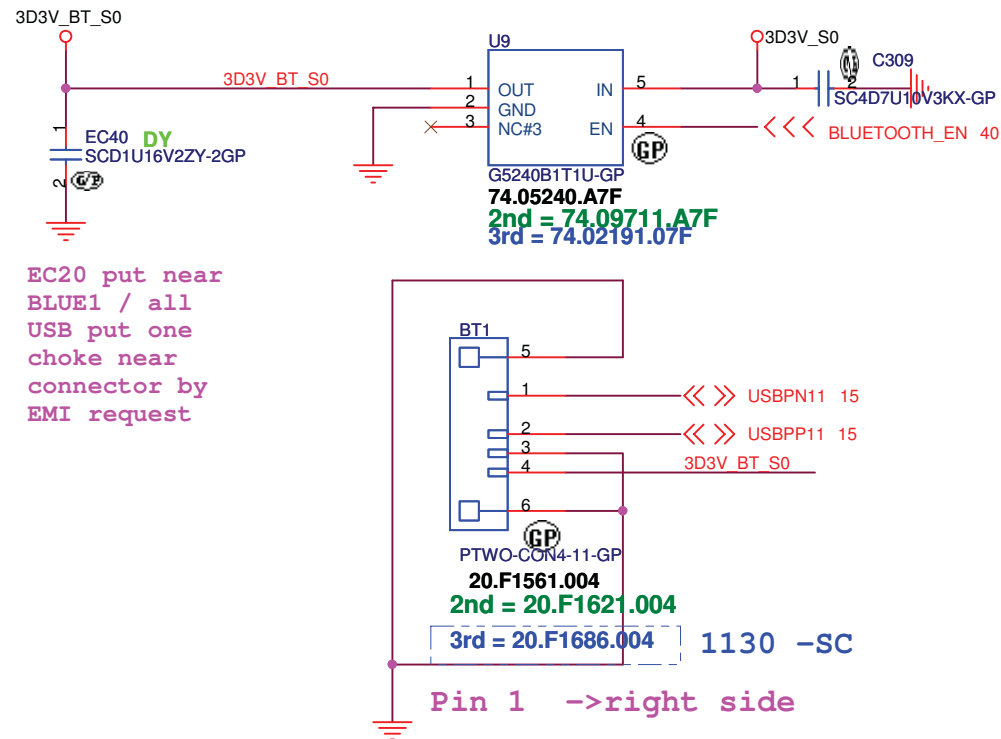
ODD Connector



UMA

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Title			
ODD			
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BLUETOOTH MODULE



JV50

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Title

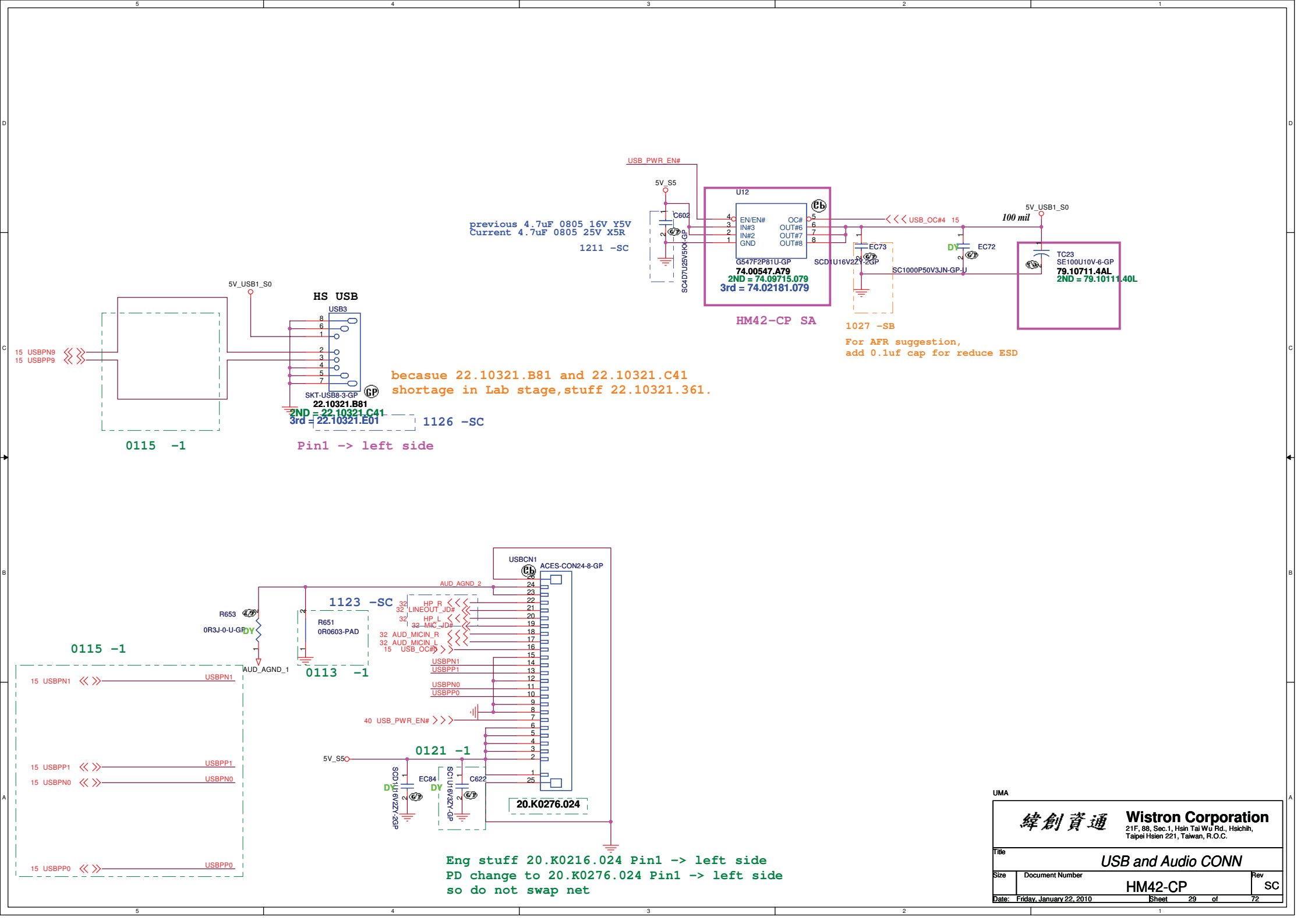
BLUETOOTH

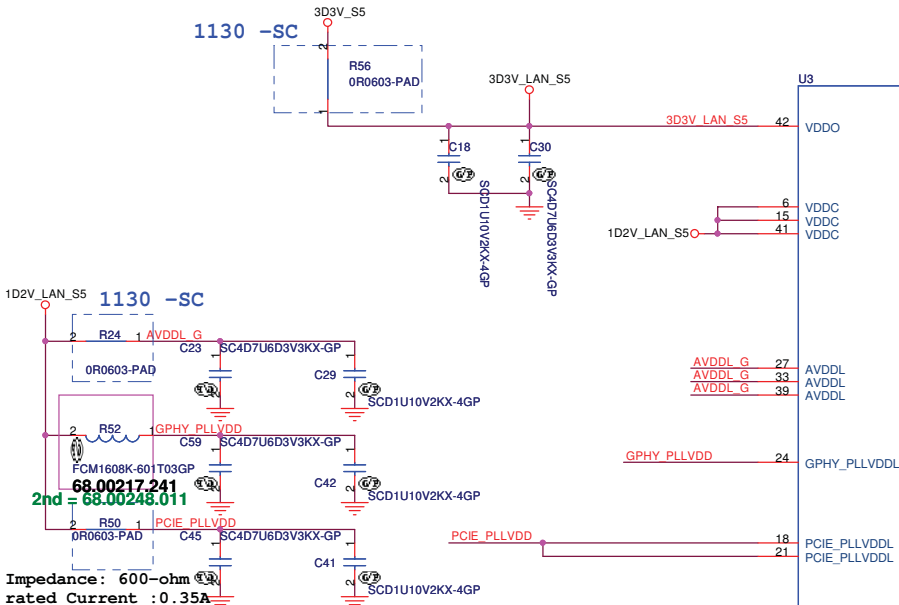
Size Document Number Rev

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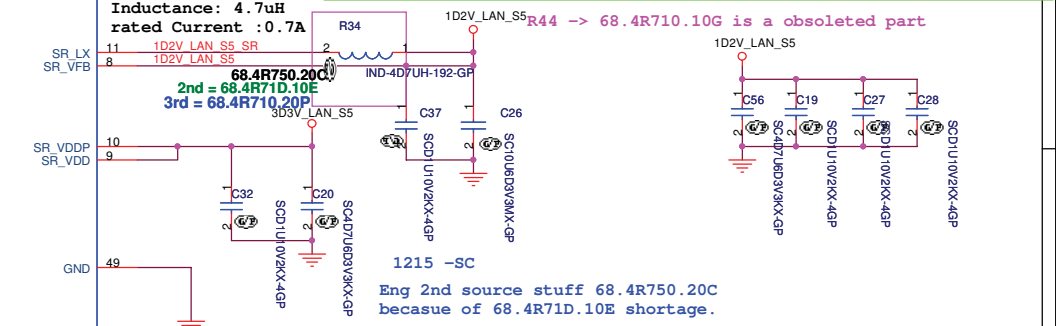
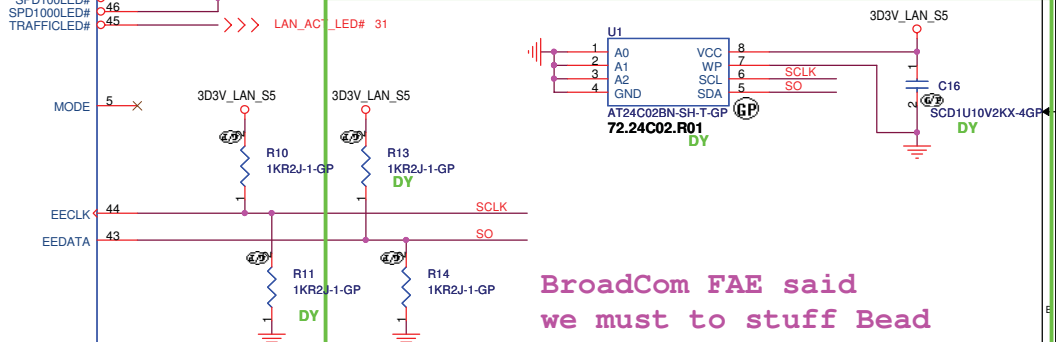
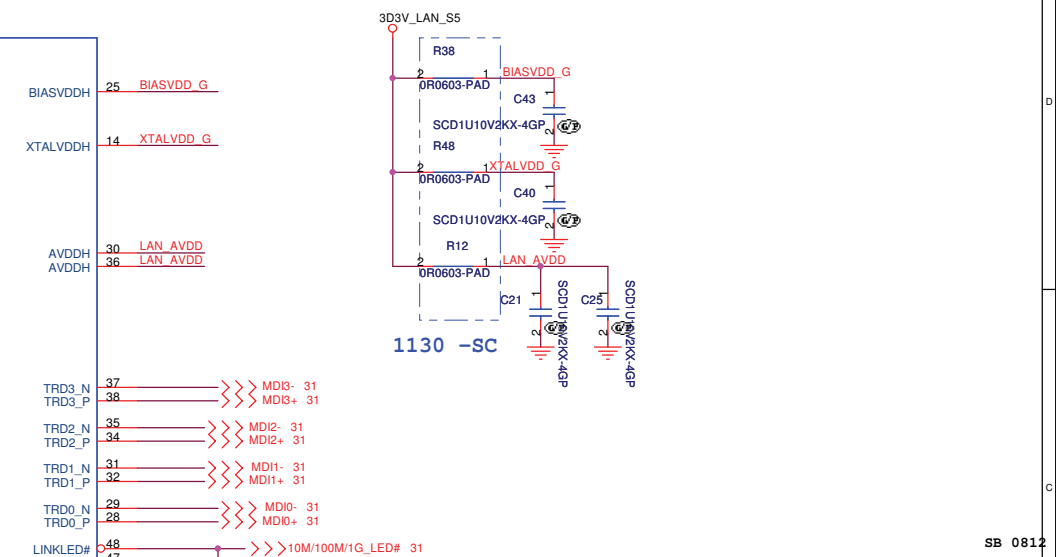
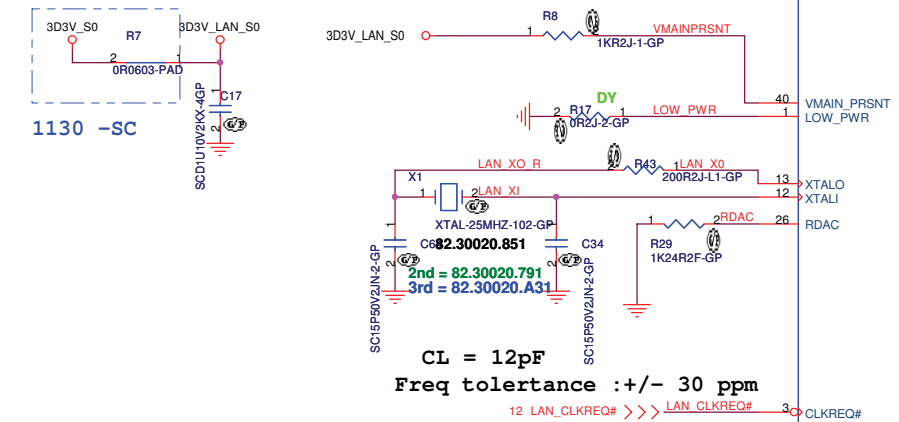
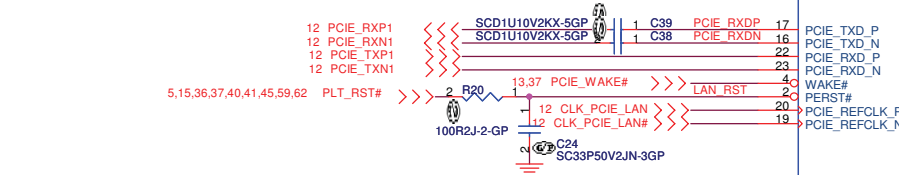
SC

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BroadCom FAE said
we must to stuff Bead



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Title
BCM57780

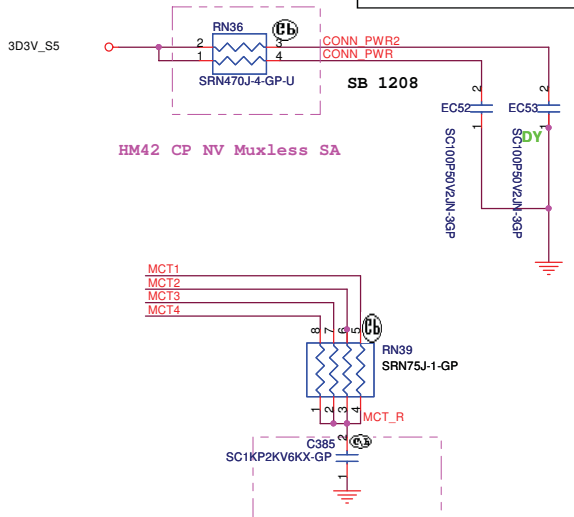
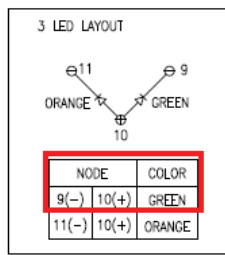
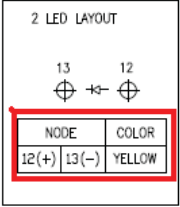
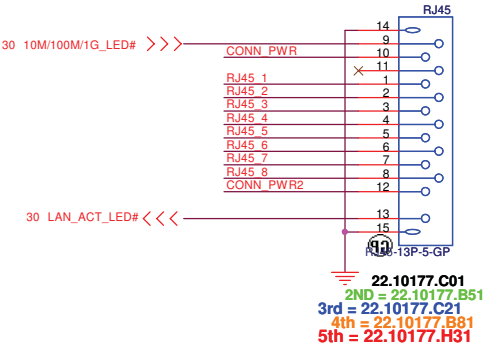
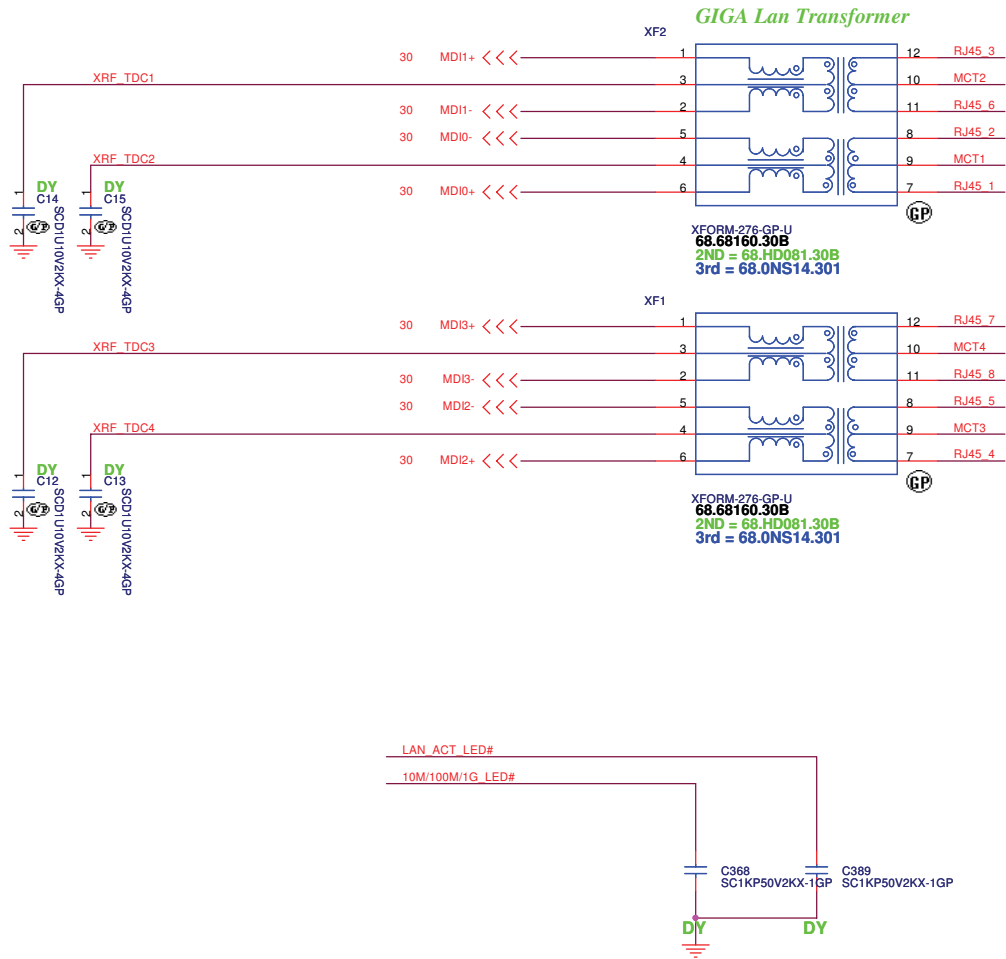
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- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Connector

LAN Connector



UMA

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Title

LAN CONN

Size A3

Document Number

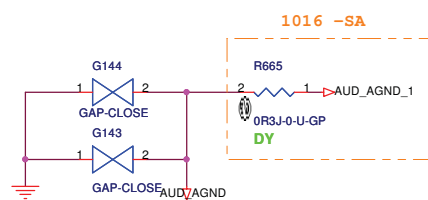
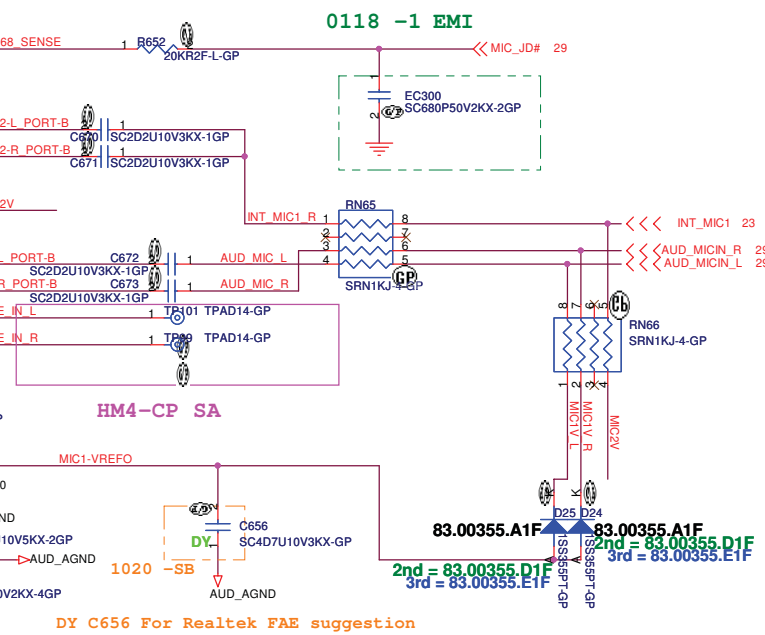
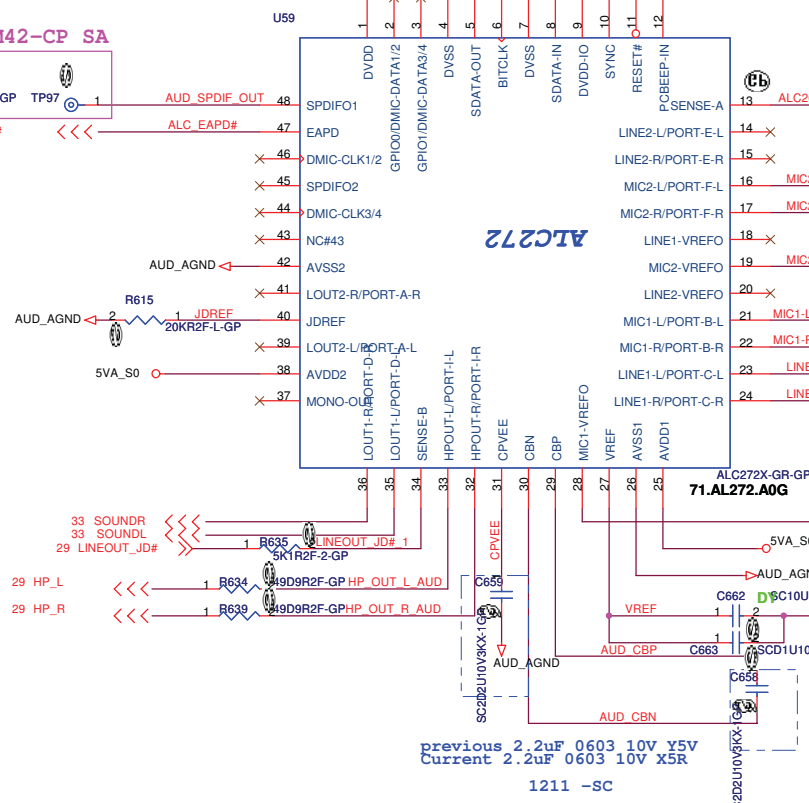
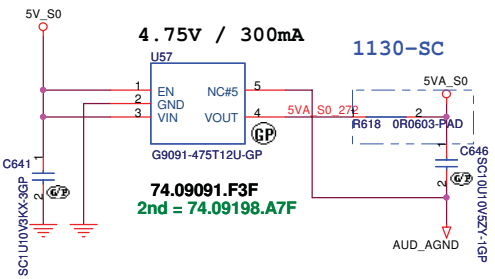
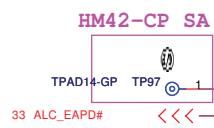
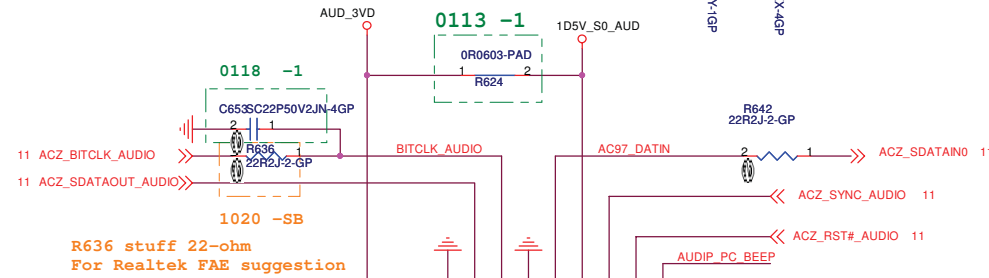
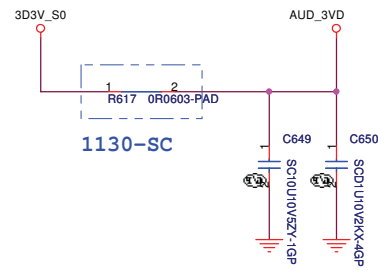
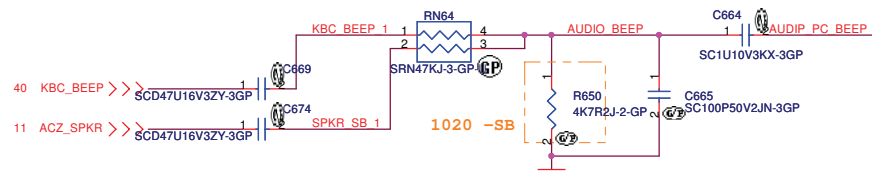
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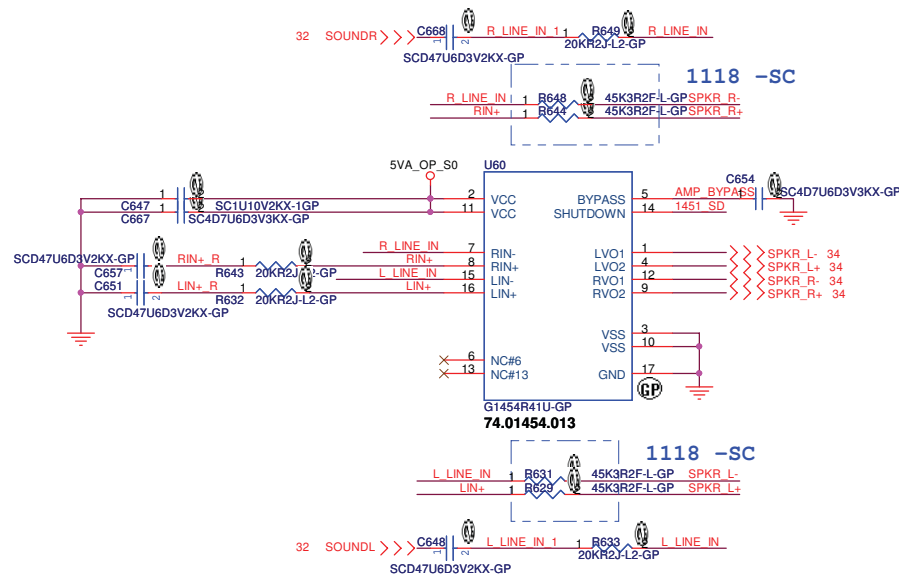
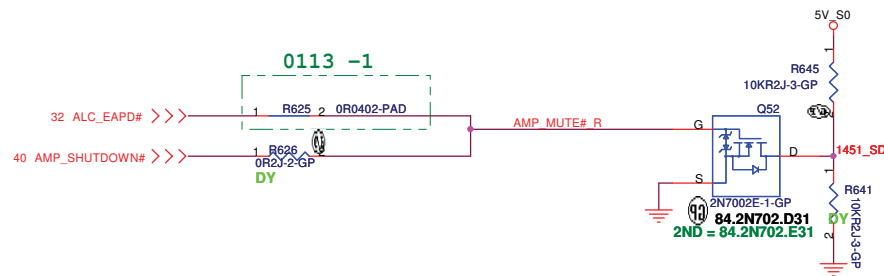
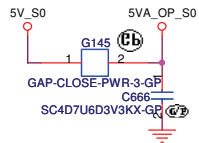
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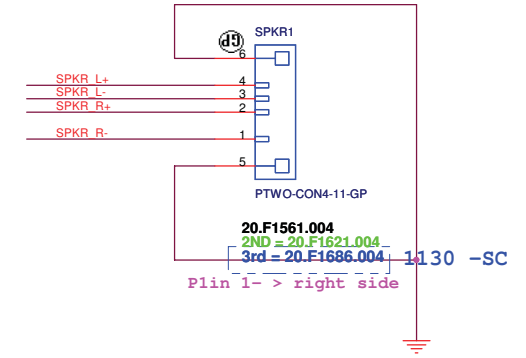
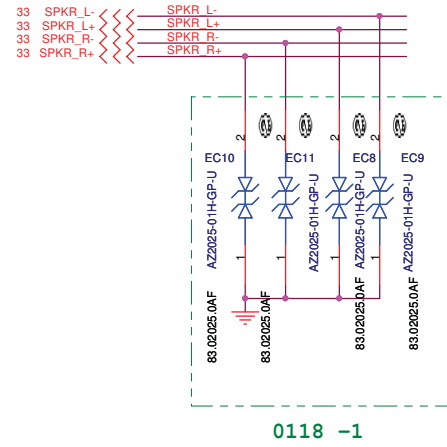
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Title Azalia codec ALC272			
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Gain= $R_f/R_i=52K/20K=2.6V/V$
 $f(HP)=1/(2 \pi * 20K * 0.47\mu f)=16.9Hz$
 If $V_{IN}=1.54V$ Gain=2.6V/V $R_L=4\Omega$ $V_O(peak)=4V$ $V(rms)=2.828V$
 Power= $2.446^2/4=1.5W$

UMA

Internal Speaker

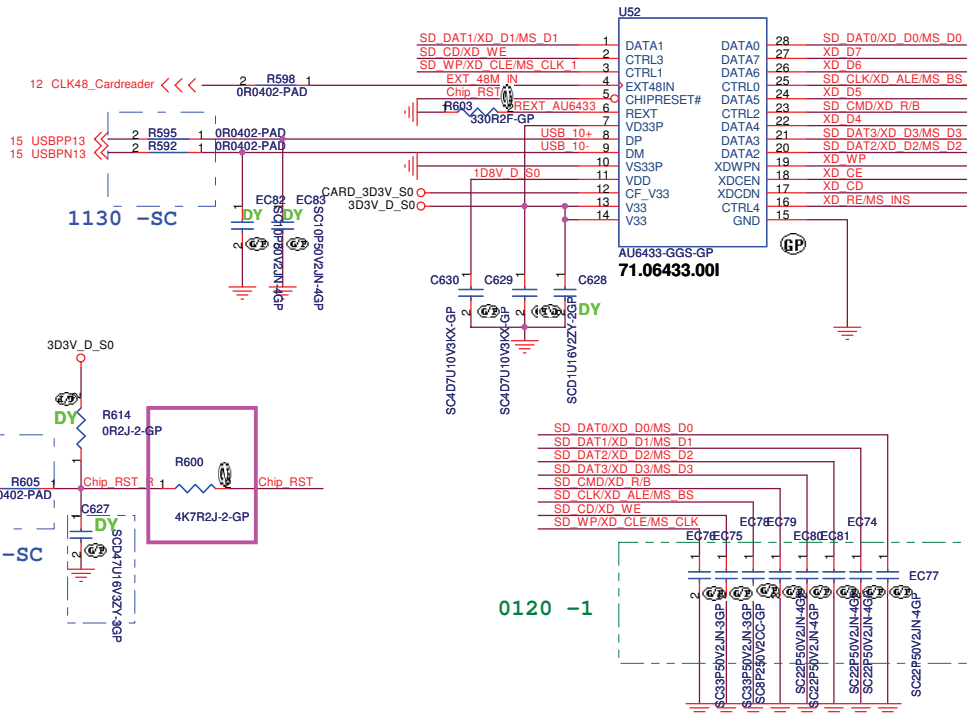
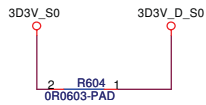


Discrete N11M

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Title			
AUDIO SPEARK			
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JV50

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Resrve MDC		
Size	Document Number	Rev
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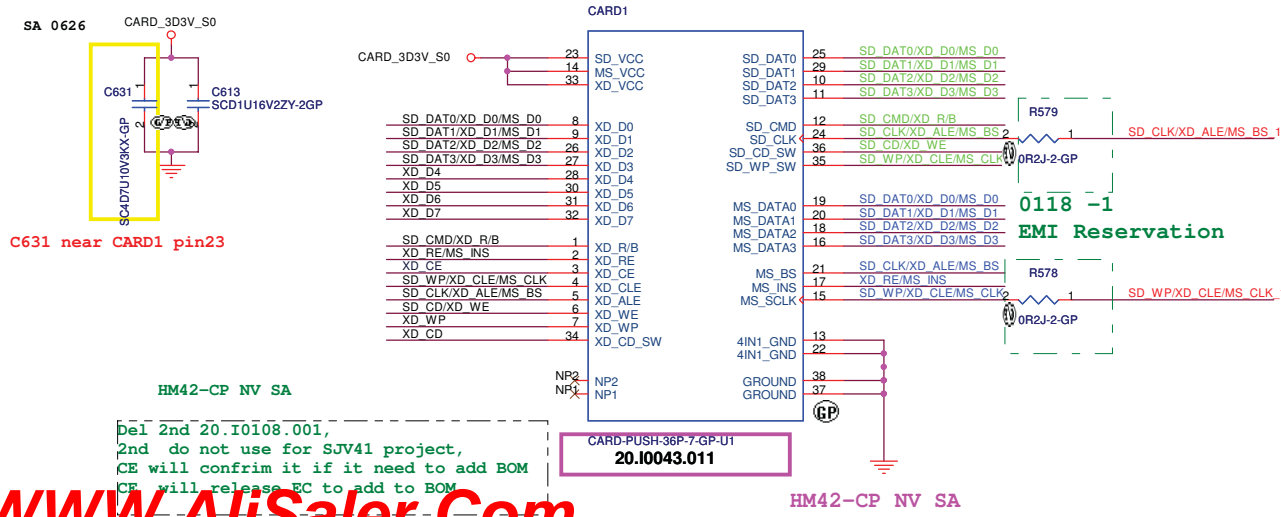


Pin	Name	SD Mode Description
1	CD/DAT3	Card detect/Data line[Bit 3]
2	CMD	Command/Response
3	VSS1	Supply voltage ground
4	VDD	Supply voltage
5	CLK	Clock
6	VSS2	Supply voltage ground
7	DAT0	Data line[Bit 0]
8	DAT1	Data line[Bit 1]
9	DAT2	Data line[Bit 2]

Pin No.	SD/MMC	MS/MS PRO	xD
P1	xD-R/B		2P
P2	xD-RE		3P
P3	xD-CE		4P
P4	xD-CLE		5P
P5	xD-ALE		6P
P6	xD-WE		7P
P7	xD-WP		8P
P8	xD-D0		10P
P9	xD-D1		11P
P10	SD-DAT2	9P	
P11	SD-DAT3	1P	
P12	SD-CMD	2P	
P13	4in1-GND	3P/6P	1P/10P
P14	MS-VCC		8P
P15	MS-SCLK		8P
P16	MS-DATA3		7P
P17	MS-INS		6P
P18	MS-DATA2		5P
P19	MS-DATA0		4P

Pin No.	SD/MMC	MS/MS PRO	xD
P20	MS-DATA1		3P
P21	MS-BS		2P
P22	4in1-GND	3P/6P	1P/10P
P23	SD-VCC	4P	
P24	SD-CLK	5P	
P25	SD-DAT0	7P	
P26	xD-D2		12P
P27	xD-D3		13P
P28	xD-D4		14P
P29	SD-DAT1	8P	
P30	xD-D5		15P
P31	xD-D6		16P
P32	xD-D7		17P
P33	xD-VCC		18P
P34	xD-CD-SW		19P
P35	SD-WP-SW	SD-WP-SW	
P36	SD-CD-SW	SD-CD-SW	
P37	4 in 1-GND	SD-WP/CD-SW-GND	
P38			

5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



Pin	Name	Dir	description
1	XD_CD#	-	presence detect
2	R/B#	OUT	Ready / Busy (open-drain)
3	RE#	IN	Read Enable
4	CE#	IN	Card Enable
5	CLE	IN	Command Latch Enable
6	ALE#	IN	Address Latch Enable
7	WE#	IN	Write Enable
8	WP#	IN	Write Protect
9	GND	-	Ground
10	SD0	IN/OUT	data bit 0
11	SD1	IN/OUT	data bit 1
12	SD2	IN/OUT	data bit 2
13	SD3	IN/OUT	data bit 3
14	SD4	IN/OUT	data bit 4
15	SD5	IN/OUT	data bit 5
16	SD6	IN/OUT	data bit 6
17	SD7	IN/OUT	data bit 7
18	VCC	-	3.3V power

Pin	Pin Name	Description
1	VSS	Vss
2	BS	Bus state signal
3	DATA1	Data1 Parallel / NC Serial
4	SDIO/DATA0	Data0 Parallel / Data Serial
5	DATA2	Data2 Parallel / NC Serial
6	INS	Stick detect (connected to VSS)
7	DATA3	Data3 Parallel / NC Serial
8	SCLK	Clock signal
9	VCC	Vcc (2.7V - 3.6V)
10	VSS	Vss

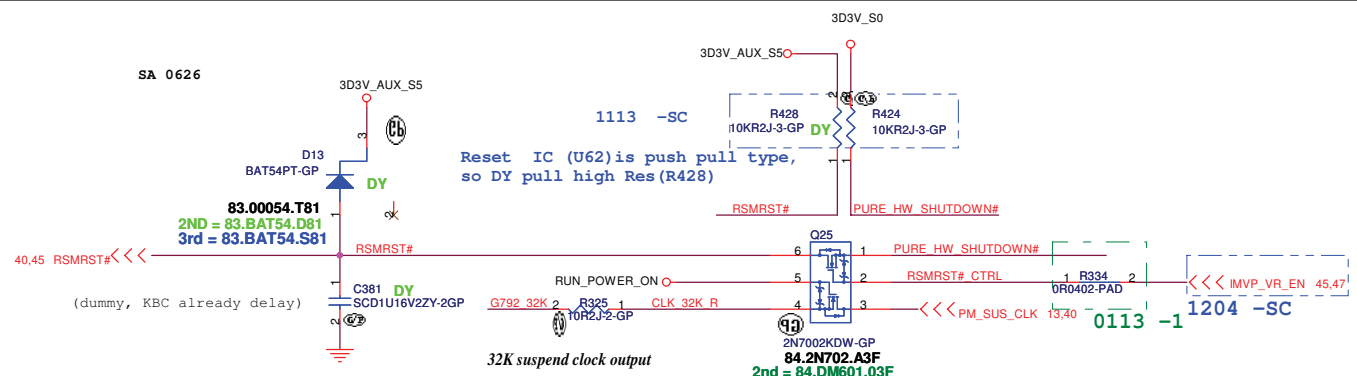
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Title: **Cardreader**

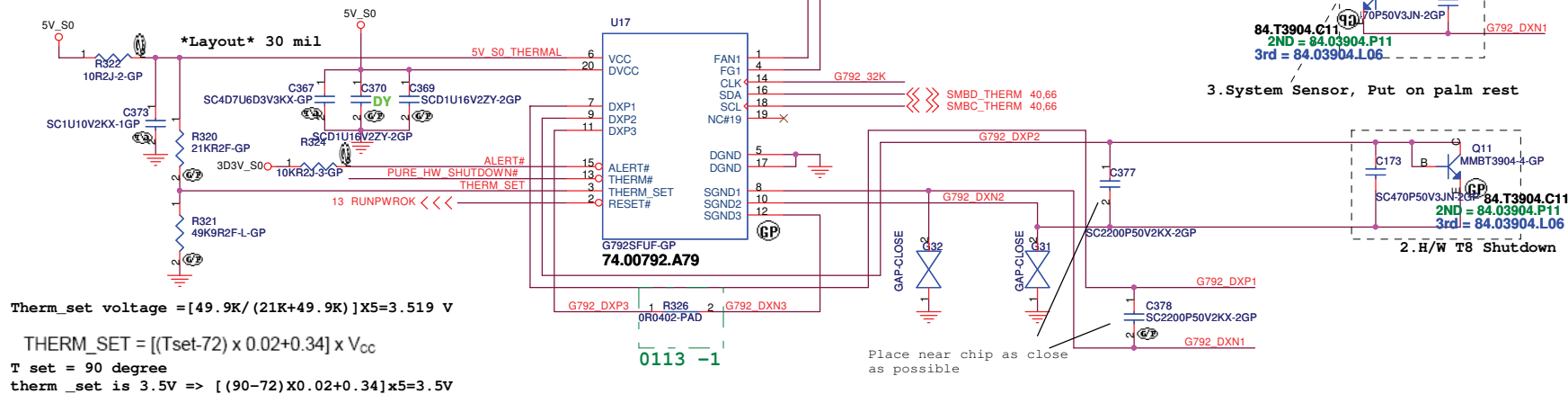
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Thermal Get define

- Sensor0 => CPU
- Sensor1=> system temp (thermal DPX1)
- Sensor2=> HW T8 shut down(thermal DPX2)
- Sensor3=> unused(thermal DPX3)
- Sensor4=> MCH
- Sensor5=> PCH
- Sensor6=> Adpater Current
- Sensor7=>dGPU
- Sensor8=>Battery Thermal
- Sensor9=>Battery Current



Therm_set voltage = $[49.9\text{K} / (21\text{K} + 49.9\text{K})] \times 5 = 3.519 \text{ V}$

$$\text{THERM_SET} = [(T_{\text{set}} - 72) \times 0.02 + 0.34] \times V_{\text{CC}}$$

T set = 90 degree

therm_set is 3.5V => $[(90-72) \times 0.02 + 0.34] \times 5 = 3.5\text{V}$

```
DXP1: System Sensor
DXP2: H/W Setting(T8)
DXP3: do not use
```

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Thermal/Fan Connector

Size

Document Number

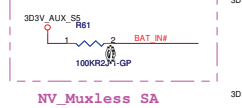
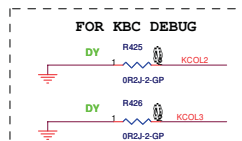
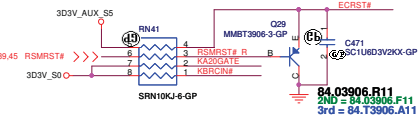
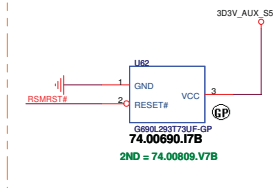
HM42-CP

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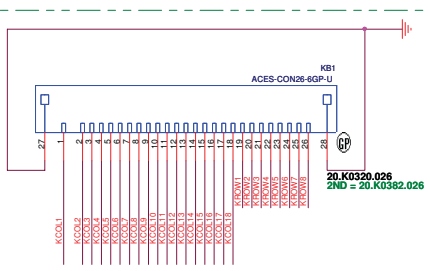
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Prevent BIOS data loss solution
1019 -SB



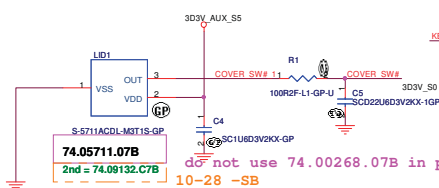
Internal Keyboard Connector



change connect to FPC (Same as Lab)
20.K0251.026 Pin 1 -> left side
20.K0320.026 Pin 1 -> right side (use in lab stage)
so swap net

0105 -1

Cover Up Switch



do not use 74.00268.07B in project for Deark suggestion

10-28 -SB

L16 -> 68.00082.011 is a obsoleted part

0930 -SA

Impedance: 60-ohm
rated Current :3A

68.00230.091
2nd = 68.00206.191

0113 -1

0113 -1

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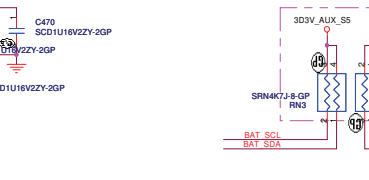
0113 -1

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0113 -1



BATTERY

THERMAL

1016 -SB

1016 -SB

1016 -SB

1016 -SB

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1016 -SB

PCB Version AID (Pin8)	Pull-Down Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	100K	10K	3.0V
SB	100K	20K	2.75V
SC	100K	30K	2.54V
-1	100K	47K	2.24V
Reserved	100K	68K	1.94V
Reserved	100K	82K	1.81V
Reserved	100K	100K	1.65V

Value	PN
10K	63.10334.1DL
8.2K	63.82234.1DL
6.98K	64.69815.6DL
4.7K	63.47234.1DL
3K	64.30015.6DL
2K	64.20015.6DL
1K	63.10234.1DL



-SA 0930

1202-SC

1 2

ER1
0R0402-PAD

R331
10KR2J-3

1021-SB

Class with KBC

```
delete 1st source(72.25105.A01)
in PD SMT
becasue it is obsolete parts
```

3D3V_AUX_S5

0113 -1

ER2
0R0603-PAD

1202 -SC

1 ER4 2 0R0402-PAD
1 ER3 2 0R0402-PAD

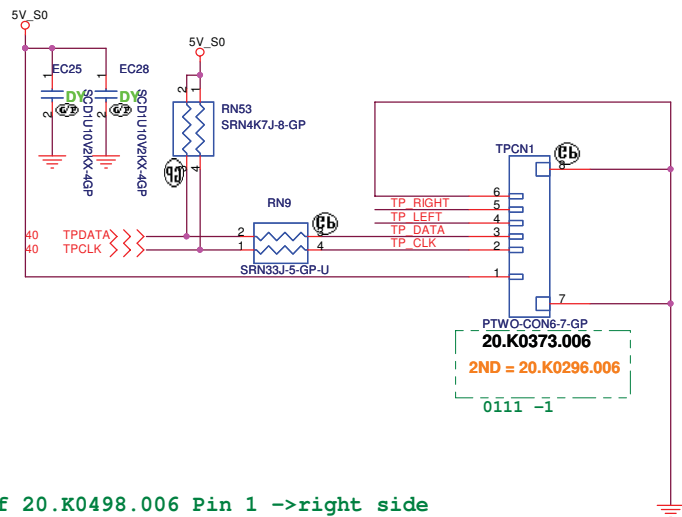
8 EC67 1 C438
6C4D7P5N1ZCN-1GP SCD1U16V2ZY2-GP

HM4-CP SA

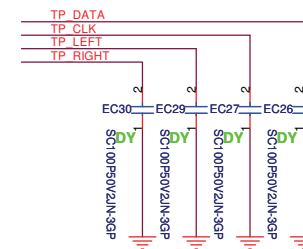
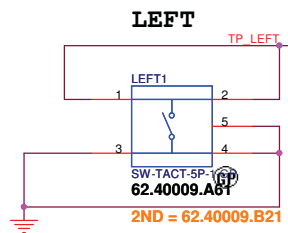
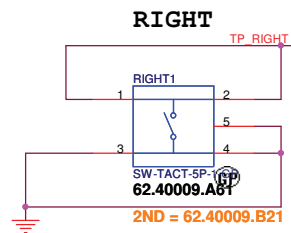
SPICKL 40
SPIDO 40

Discrete N11M

Title			
BIOS			
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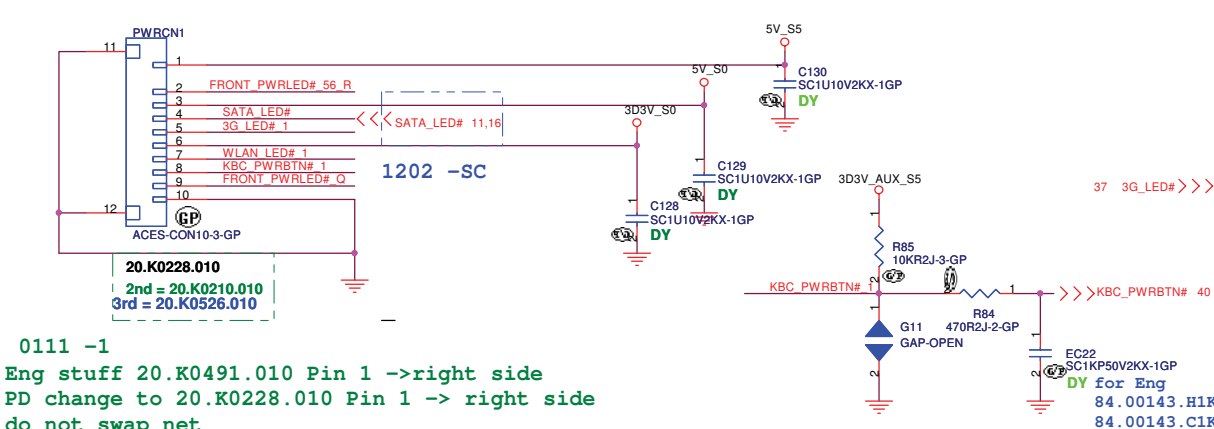
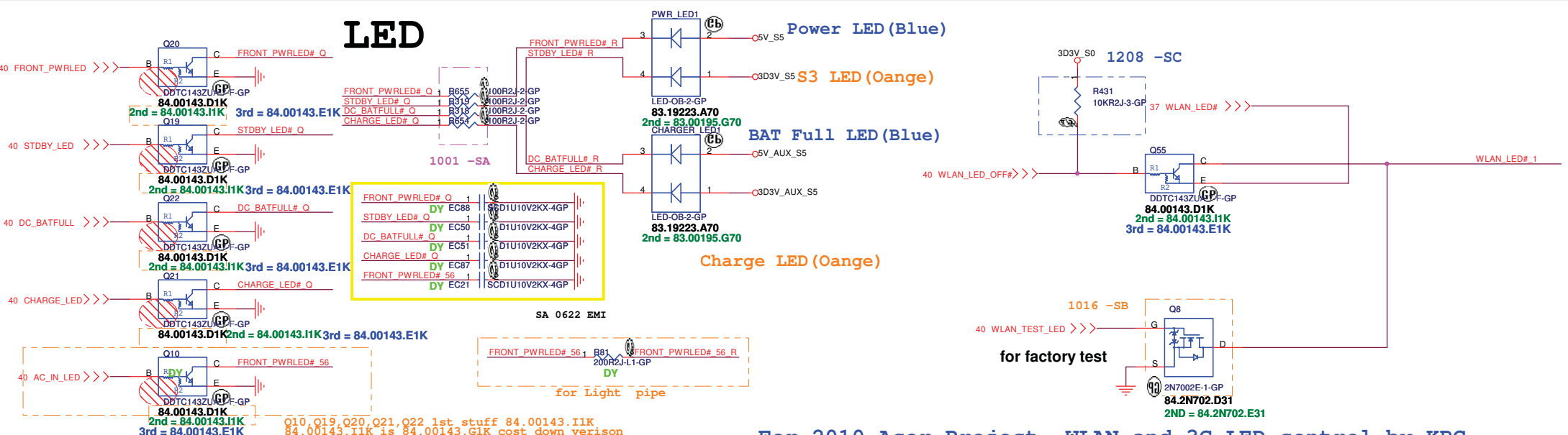
Eng stuff 20.K0498.006 Pin 1 ->right side
PD change to 20.K0373.006 pin 1 ->left side
so net mirror Vertically



Discrete N11M

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Title Touch PAD			
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LED



0111 -1
Eng stuff 20.K0491.010 Pin 1 ->right side
PD change to 20.K0228.010 Pin 1 -> right side
do not swap net

Pin 1	5V_S5	
Pin 2	FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	MEDIA_LED#_R	HDD
Pin 5	3G_LED#_R	3G
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	FRONT_PWRLED#_Q	Power LED
Pin 10	GND	

	WLAN_LED_OFF#	WLAN_TEST_LED	WWAN_LED
WLAN ON Always on	L	H	L
WLAN ON (flash)	H	L	L
WWAN_ON	L	L	H
WLAN ON WWAN_ON	L	L	H

<Core Design>

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Title: **LED&POWERBD CONN**

Size: Document Number: **HM42-CP** Rev: SC

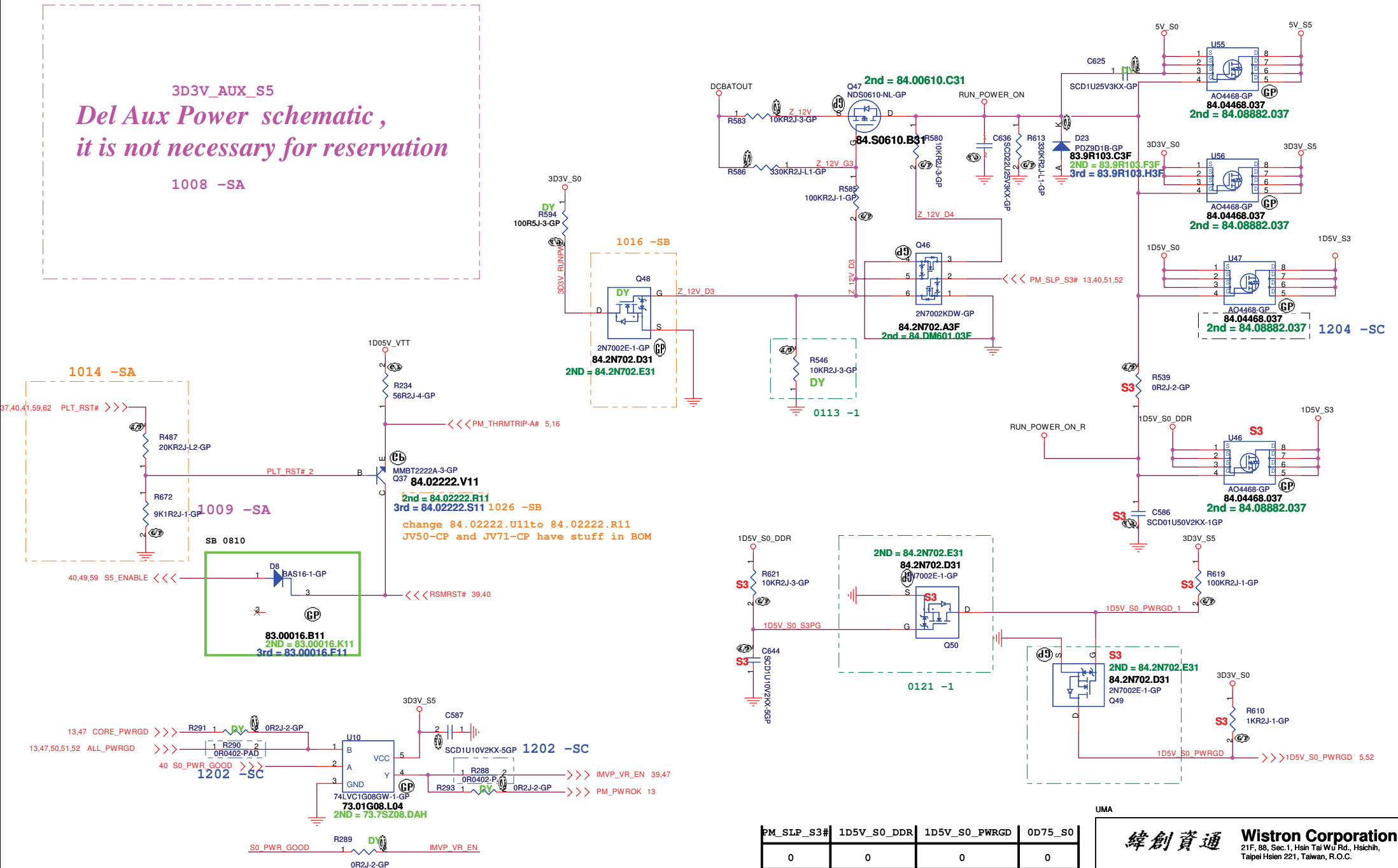
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Run Power

3D3V_AUX_S5

*Del Aux Power schematic ,
it is not necessary for reservation*

1008 -SA



PM_SLP_S3#	1D5V_S0_DDR	1D5V_S0_PWRGD	0D75_5
0	0	0	0
1	1	1	1

UMA

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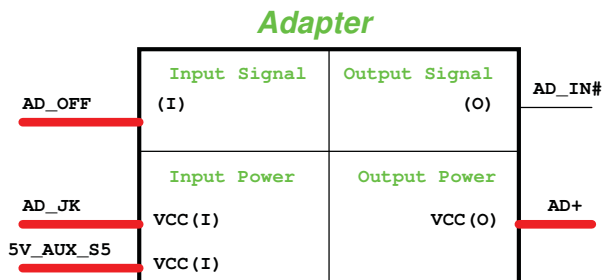
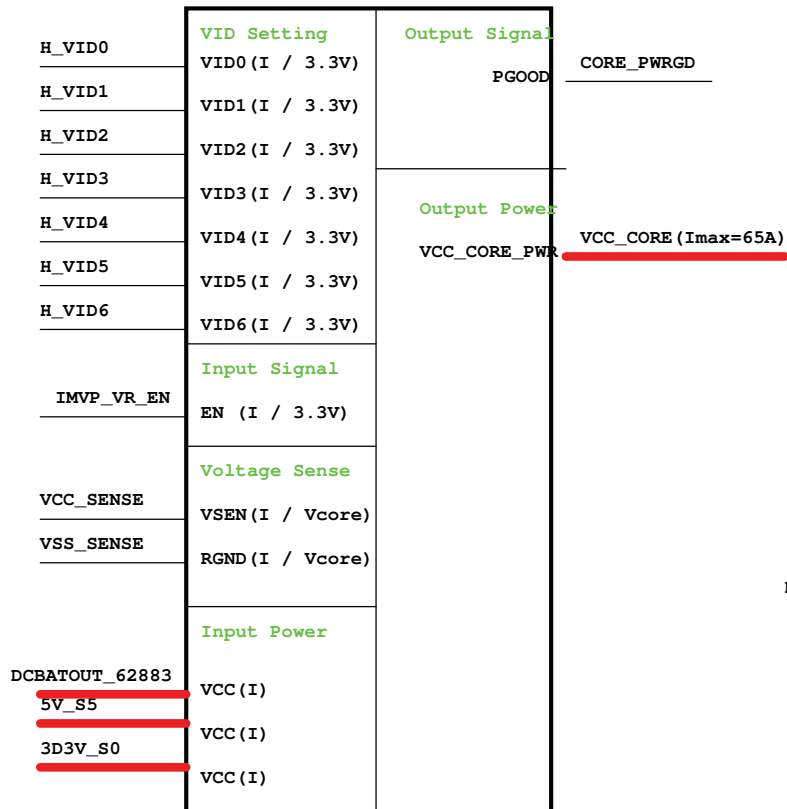
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<i>RUN POWER and 3D3V AUX S5</i>		
Size	Document Number	Rev

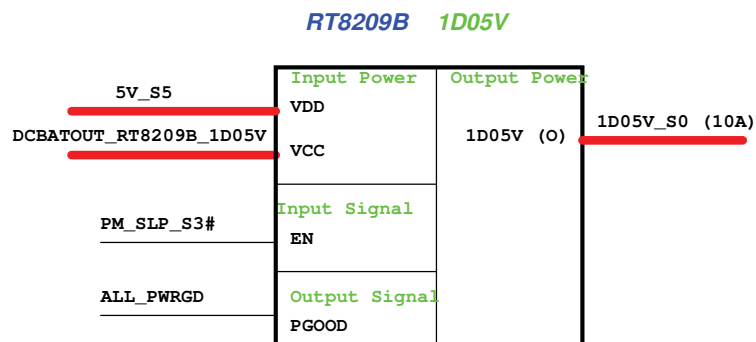
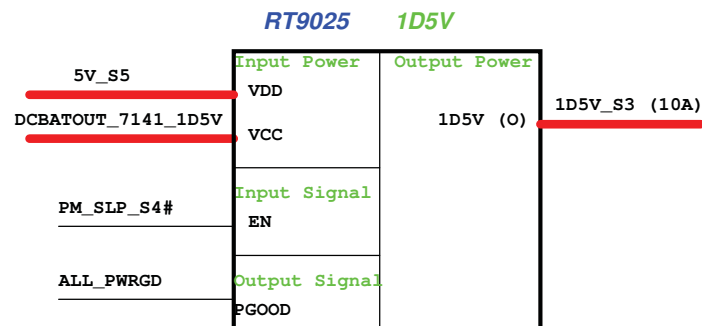
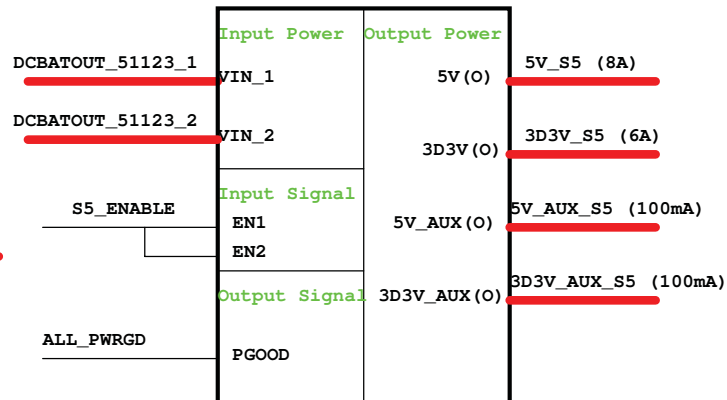
Part	Equipment	SC
	HM42-CP	SC

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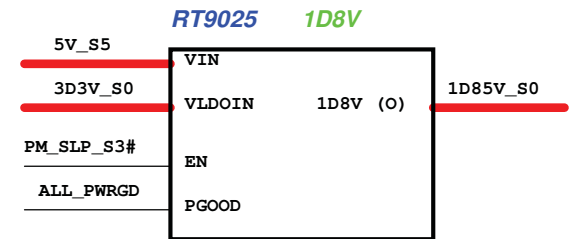
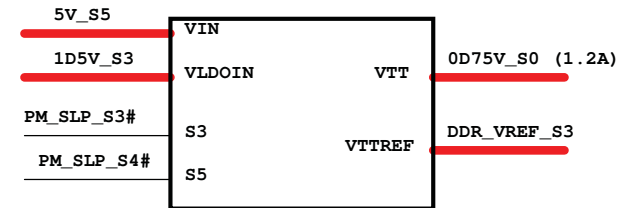
ISL62883 VCC_CORE



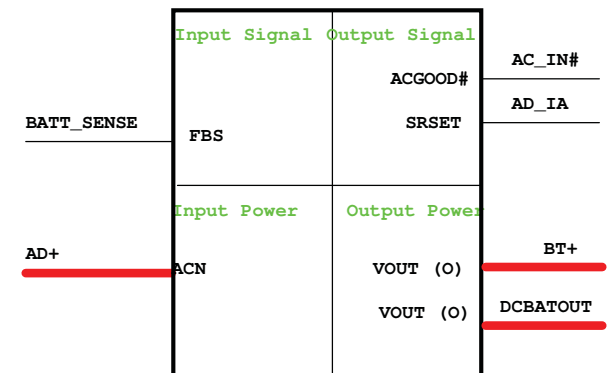
TPS51123 5V/3D3V



RT9026 0D75V_S0



Charger BQ24745



Discrete N11M

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Title

Power Block Diagram

Size

Document Number

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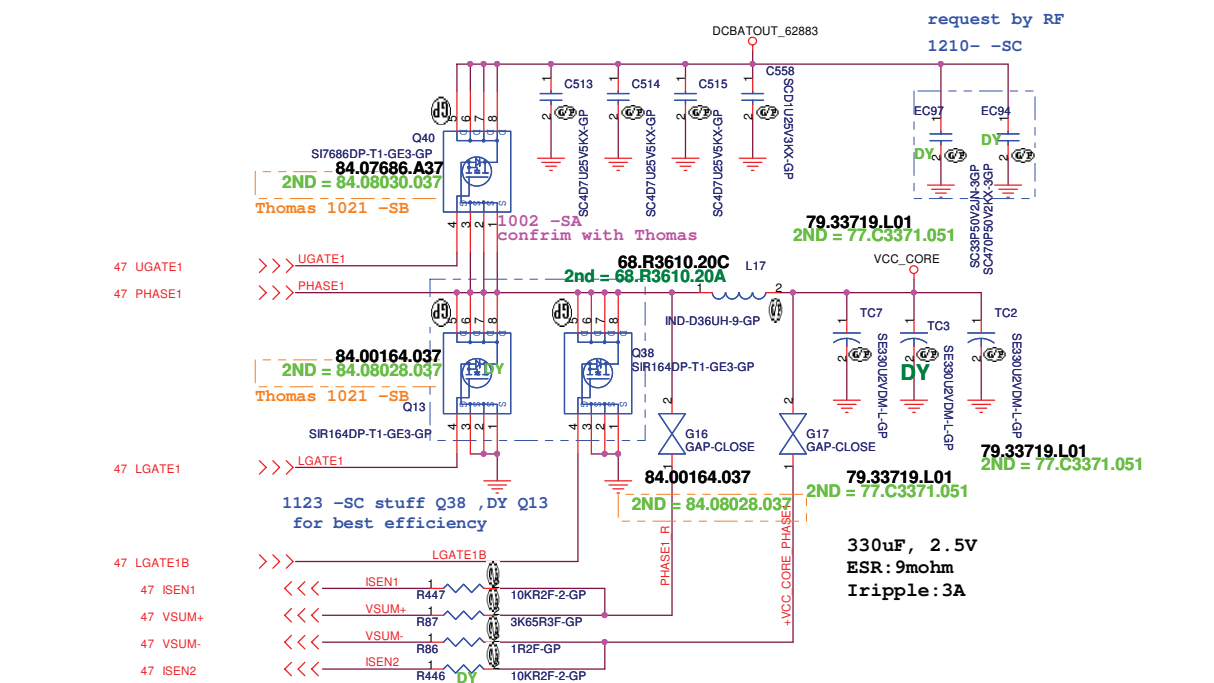
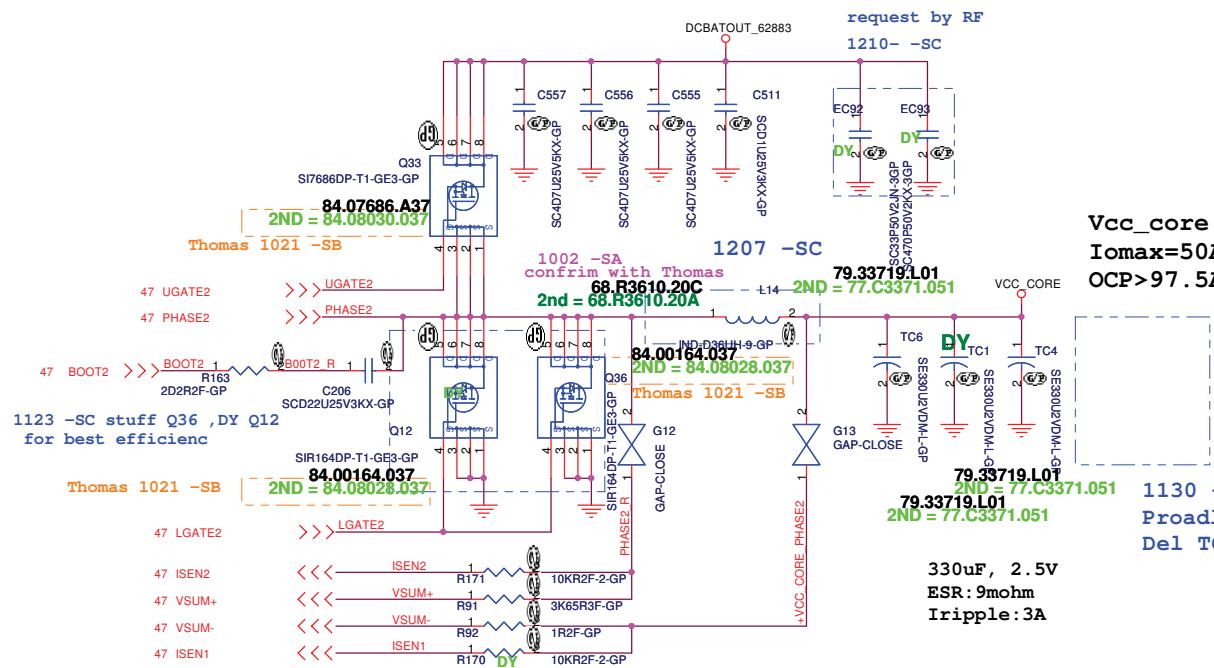
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SC

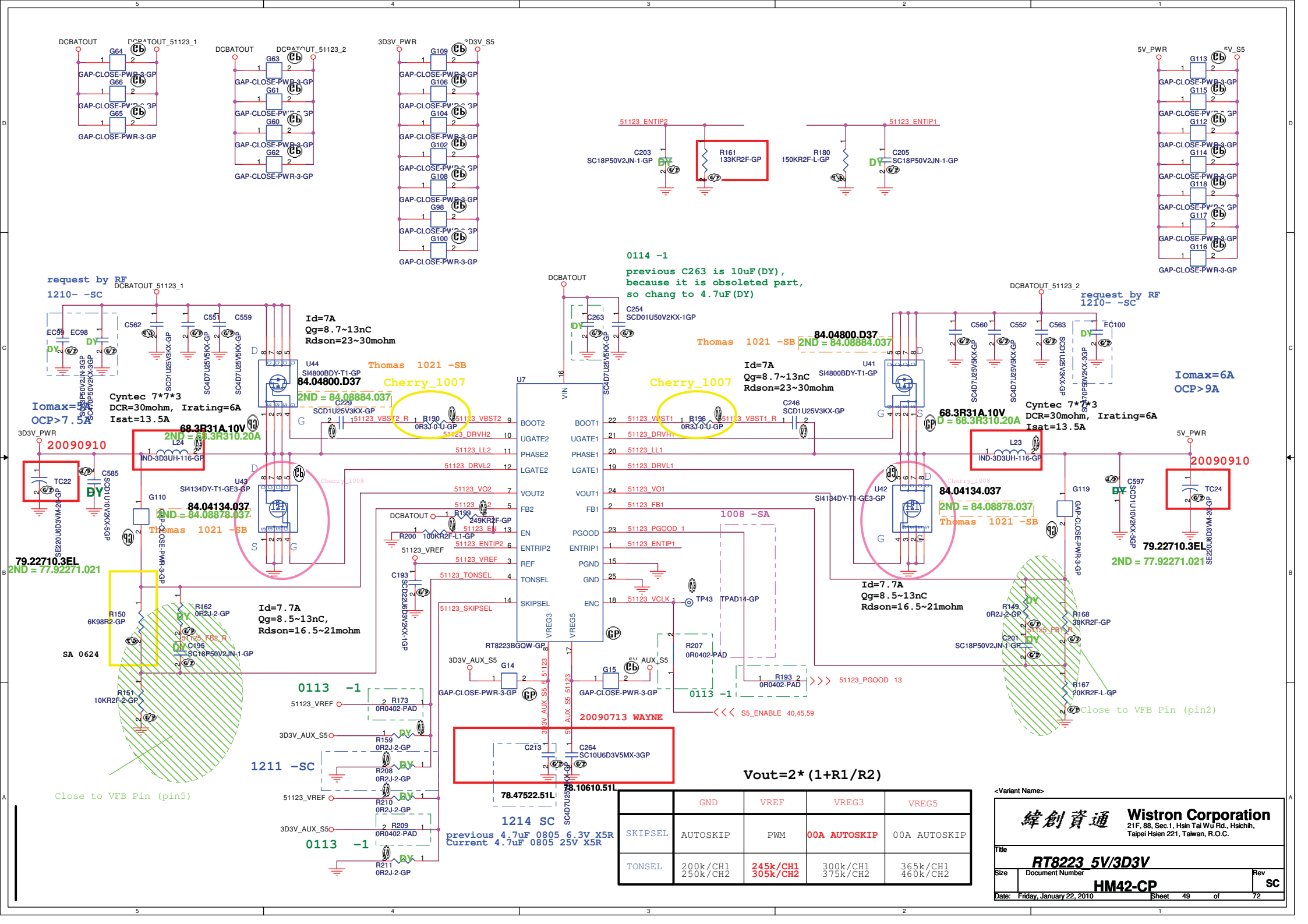
HM42-CP



1130 -SC
Broadlizer Cap power team testing fail,
Del TC5 for co-layout

330uF, 2.5V
ESR: 9mohm
Iripple: 3A

330uF, 2.5V
ESR: 9mohm
Iripple: 3A



0114 -1
previous C263 is 10uF (DY),
because it is obsoleted part,
so change to 4.7uF (DY)

Thomas 1021 -SB 2ND = 84.08884.037

Id=7A
Qg=8.7~13nC
Rdson=23~30mohm

Cherry_1007

68.3R31A.10V
D = 68.3R310.20A

Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A

Iomax=6A
OCP>9A

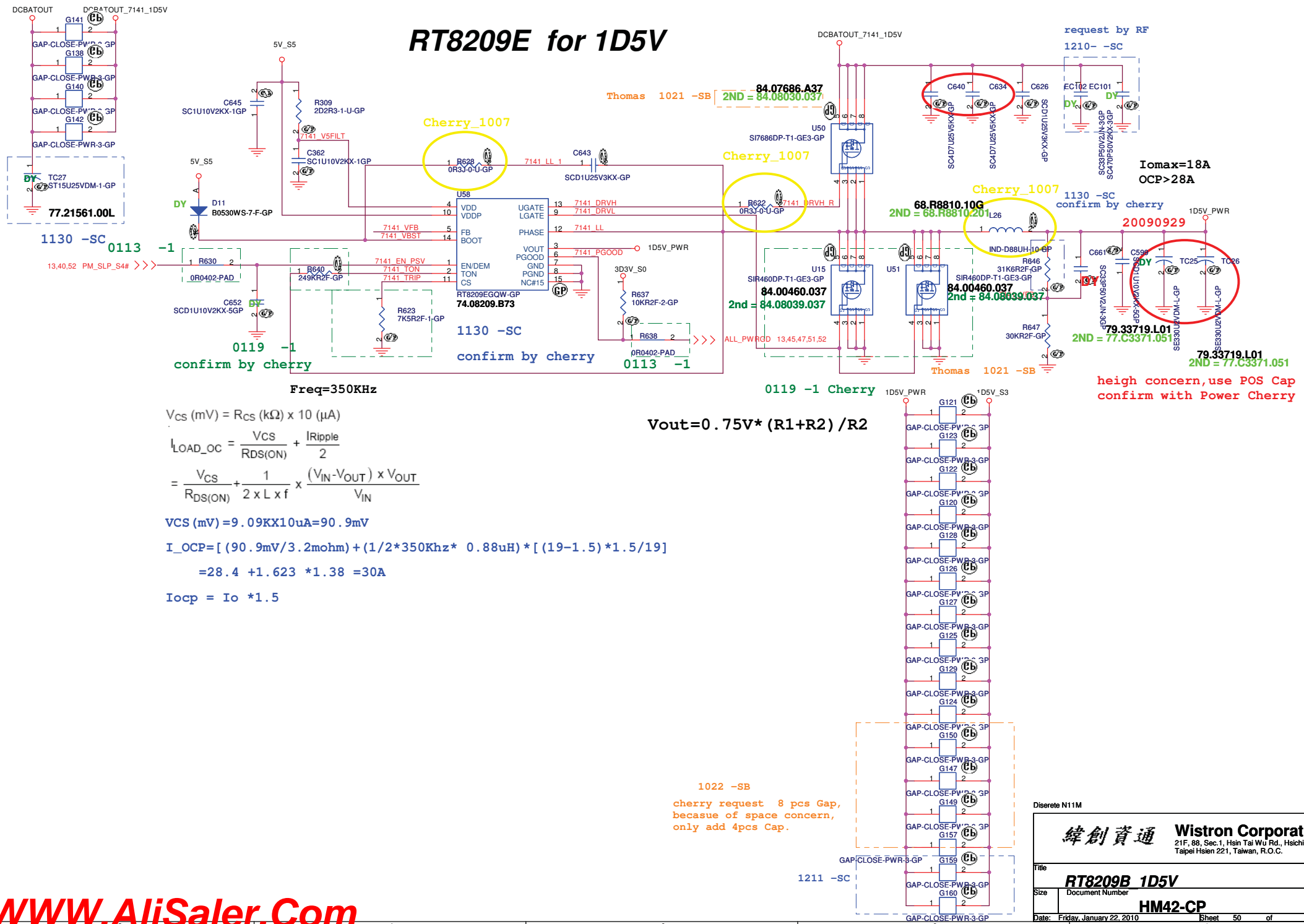
$$V_{out} = 2 * (1 + R1/R2)$$

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

<Variant Name>

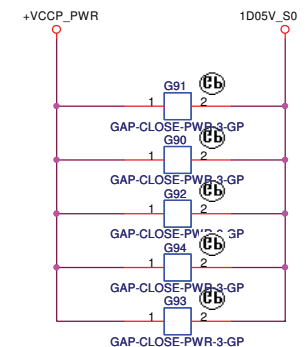
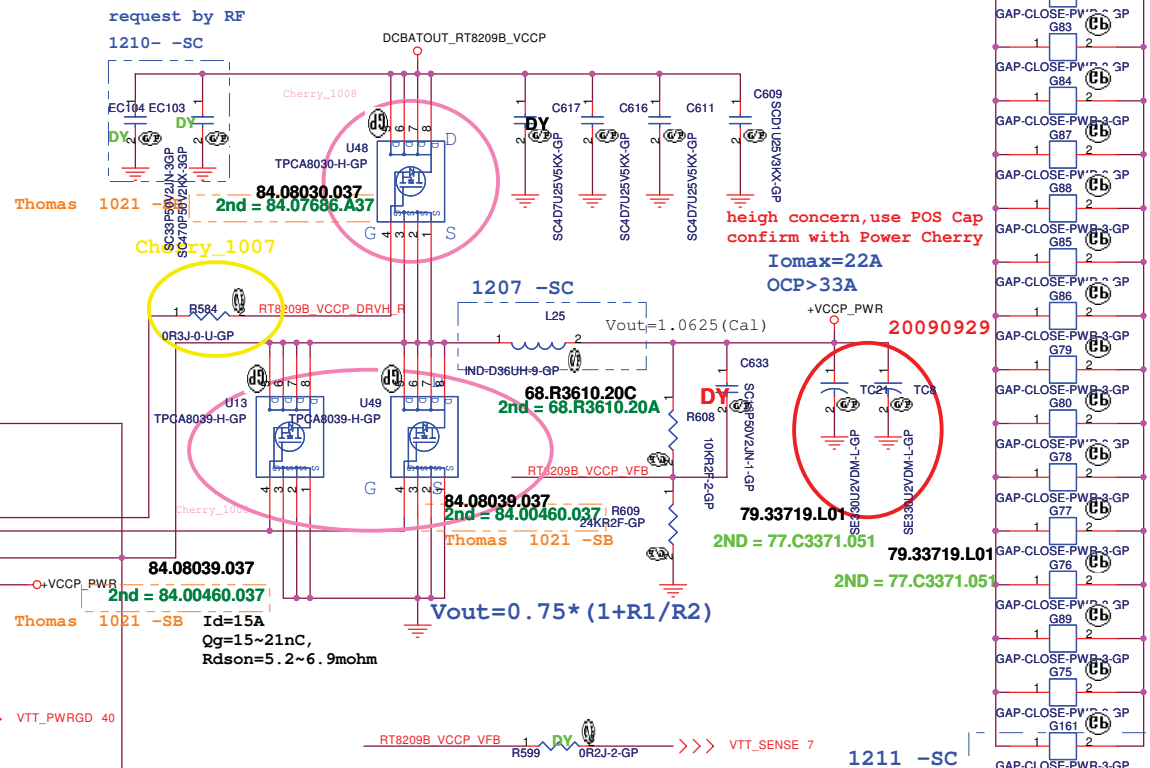
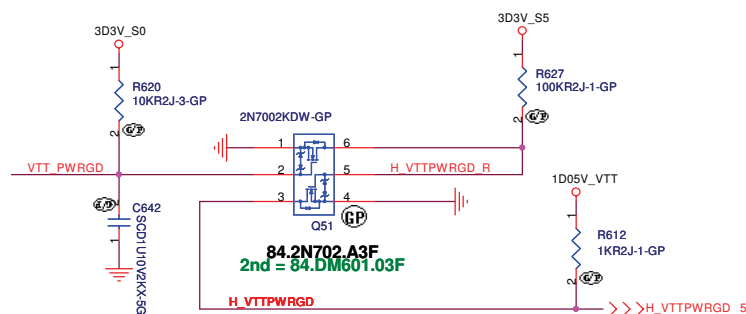
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Title RT8223 5V/3D3V	
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RT8209E for 1D5V



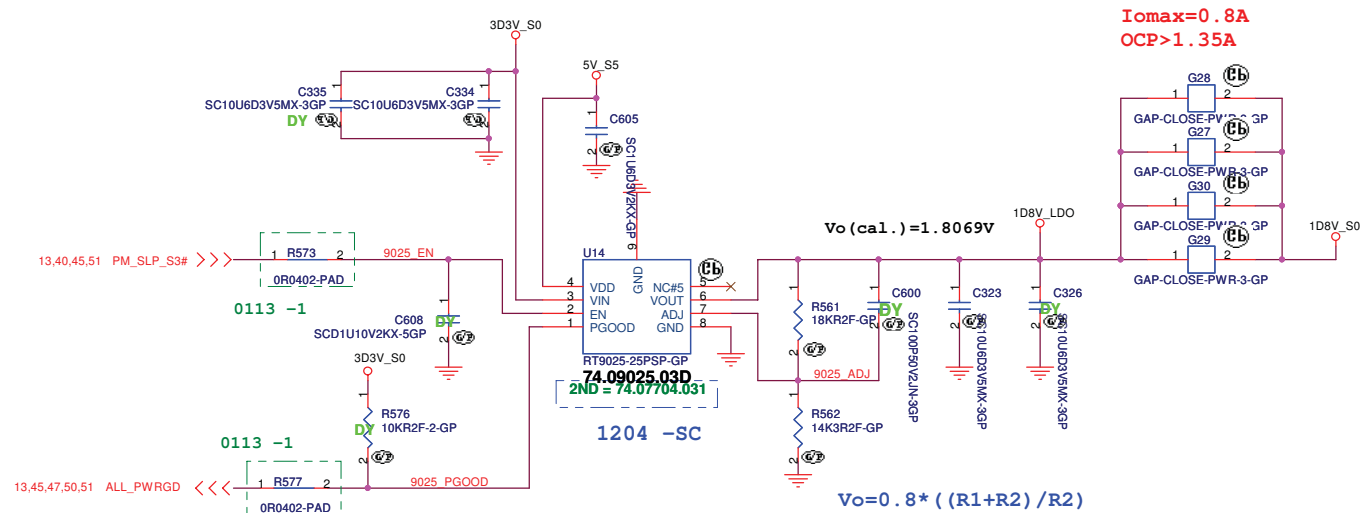


becasue of 1.05V_S0 and 1.05V_VTT combin together
use PM_SLP_S3# Enable 1.05V power

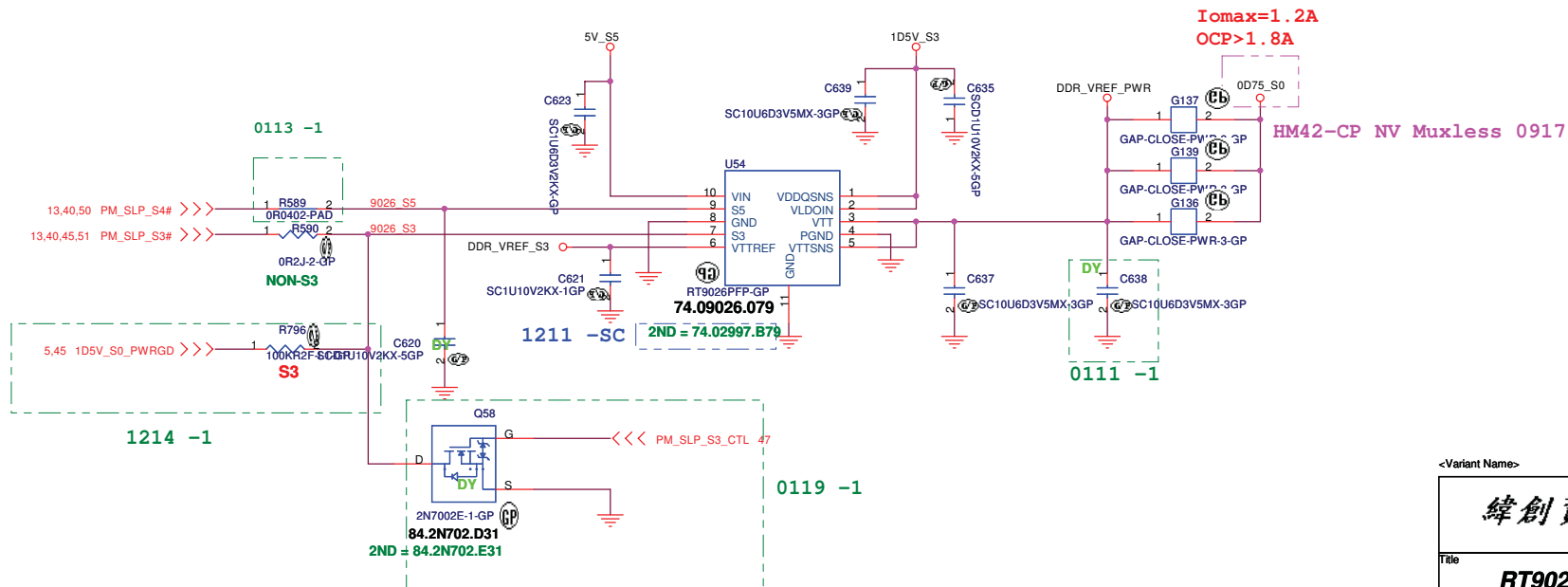


RT9025 for 1D8V_S0

20090915



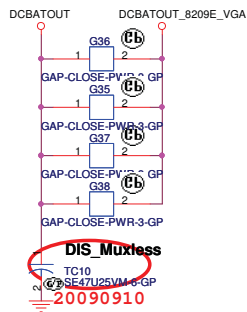
RT9026 for 0D75V_S0



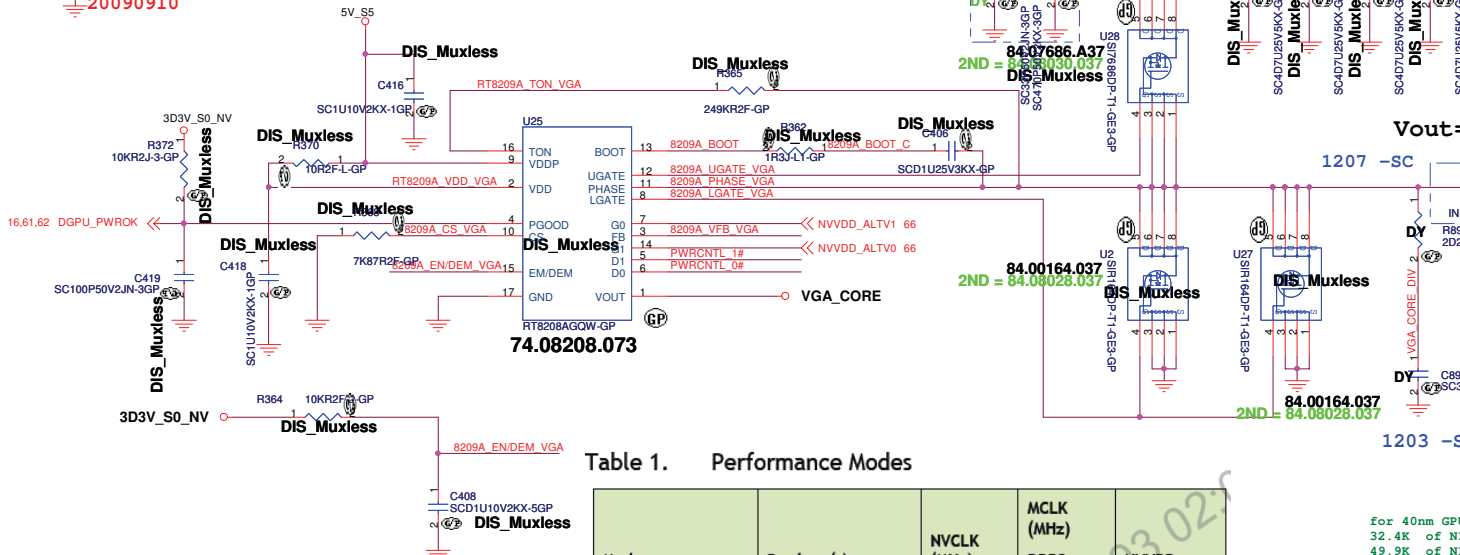
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RT8208A for VGA



RT8208A		RT8208B		Output Voltage Equation
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2/R3)}{(R2/R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2/R4)}{(R2/R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2/R3/R4)}{(R2/R3/R4)} \times 0.75$

I_{omax}=27A
OCP>40A

$$V_{out} = 0.75V * (R1+R2) / R2$$

68.R3610.20C
2nd = 68.R3610.20A

VGA_CORE

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVD
Performance (P0)	N11M-OP1	625	790	1.03 V
Performance (P0)	N11M-OP2	525	700	0.86 V
Balanced (P8)	N11M-OP1 N11M-OP2	405	405	0.85 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVD
Performance (P0)	N11P-GE1	575	790	0.95 V
Performance (P0)	N11P-LP1	475	700	0.85 V
Balanced (P8)	N11P-GE1 N11P-LP1	405	324	0.85 V
Battery (P12)	N11P-GE1 N11P-LP1	135	135	0.80 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVD
Performance (P0)	N11M-GE1	625	790	1.03 V
Performance (P0)	N11M-LP1	525	700	0.86 V
Balanced (P8)	N11M-GE1 N11M-LP1	405	405	0.85 V
Battery (P12)	N11M-GE1 N11M-LP1	135	135	0.85 V

N11P-GE1
For 40nm GPU the NVVD and GPIO5 (NVVD_ALTV0) /GPIO6 (NVVD_ALTV1) relationship

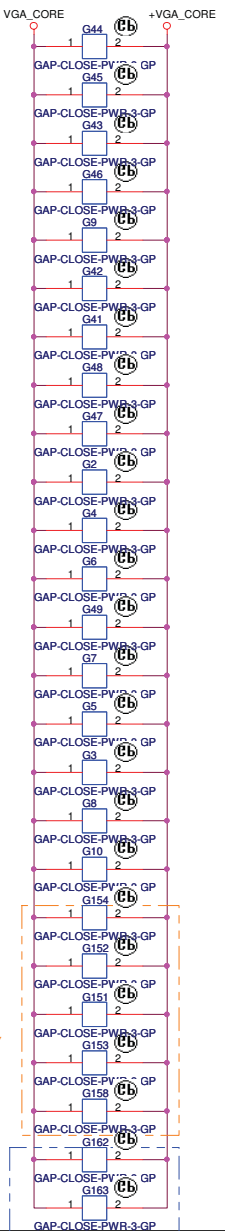
GPIO6/NVVD_ALTV1	GPIO5/NVVD_ALTV0	NVVD
0	0	0.8
0	1	0.85
1	0	0.95

N11M-GE1/N11M-OP1

For 40nm GPU the NVVD and GPIO5 (NVVD_ALTV0) /GPIO6 (NVVD_ALTV1) relationship

GPIO6/NVVD_ALTV1	GPIO5/NVVD_ALTV0	NVVD
0	1	0.85
1	0	1.03

cherry request 9 pcs Gap, because of space concern, only add 5pcs Cap.



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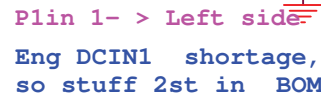
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

RT8209A VGA CORE

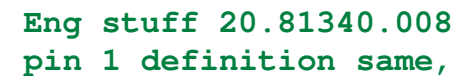
HM42-CP

Date: Friday, January 22, 2010

AD_JK Eng D14,D15 3td shortage,
so stuff 1st in BOM



BATTERY CONNECTOR



1 ^o	GND ^o	<u>Batt-</u> , Battery Negative Terminal ^o
2 ^o	GND ^o	<u>Batt-</u> , Battery Negative Terminal ^o
3 ^o	SMD ^o	SMBus data interface I/O pin ^o
4 ^o	SMC ^o	<u>SMBus</u> clock interface I/O pin ^o
5 ^o	TH ^o	Connect to Resistor to GND (10kΩ to GND) ^o
6 ^o	BI ^o	System present pin, low active ^o
7 ^o	BATT+ ^o	<u>Batt+</u> , Battery Positive Terminal ^o
8 ^o	BATT+ ^o	<u>Batt+</u> , Battery Positive Terminal ^o

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AD/BATT CONN

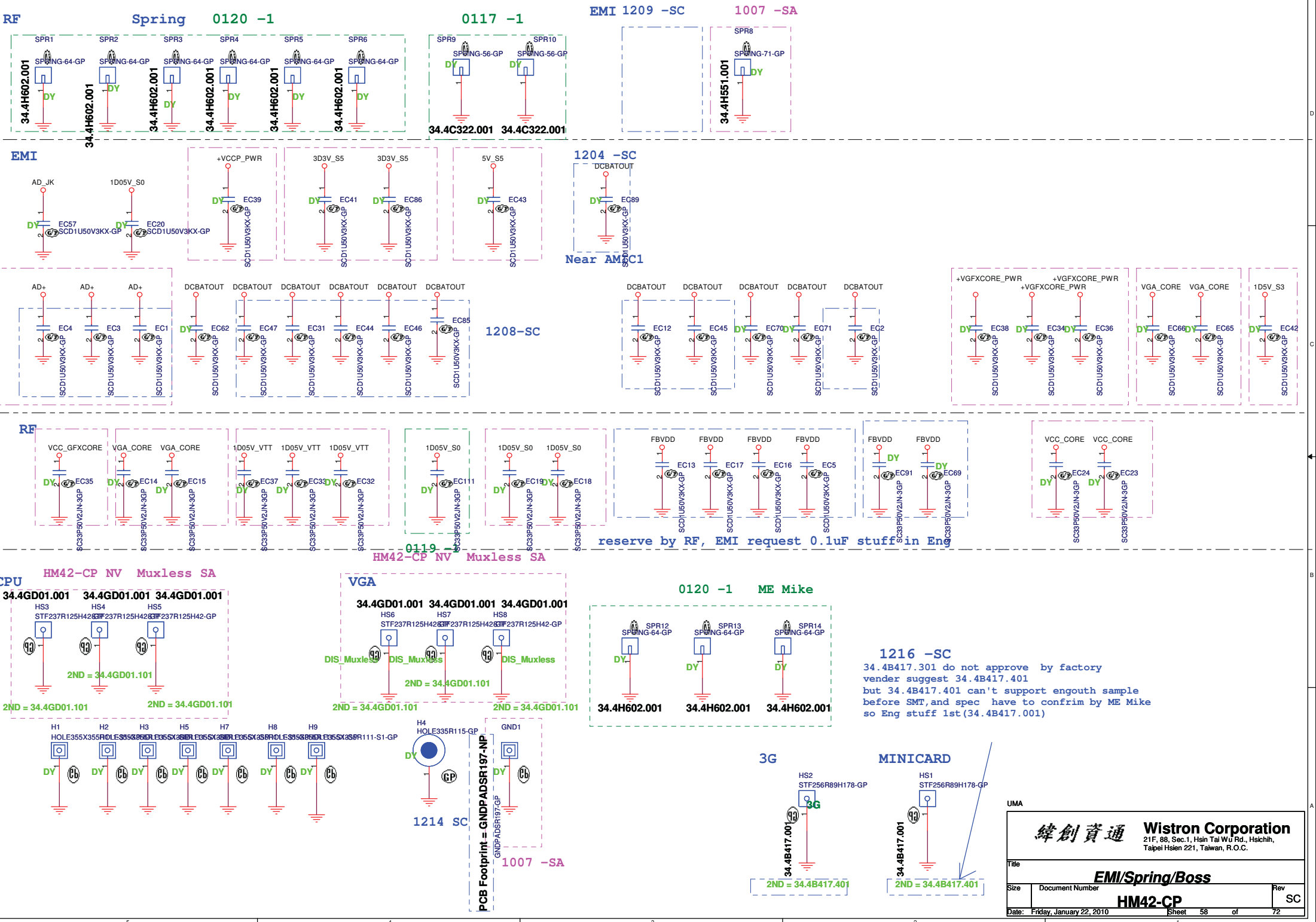
HM42-CP

SC

Date: Friday, January 22, 2010

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72



Check test point

~~delete 3D3V_S0 test point~~



Test Point放在Dimm Door打開可量測處

<Variant Name>

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Title

AFTE TP

Size

Document Number

HM42-CP

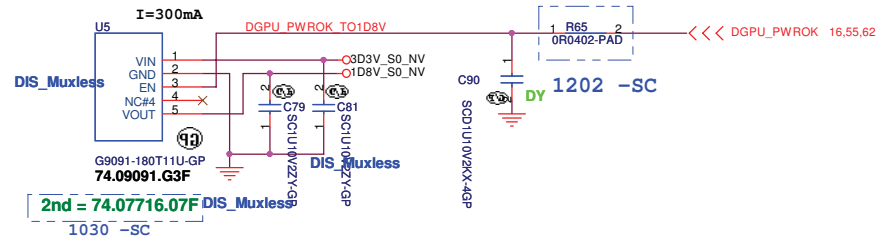
Rev

SC

Date: Friday, January 22, 2010

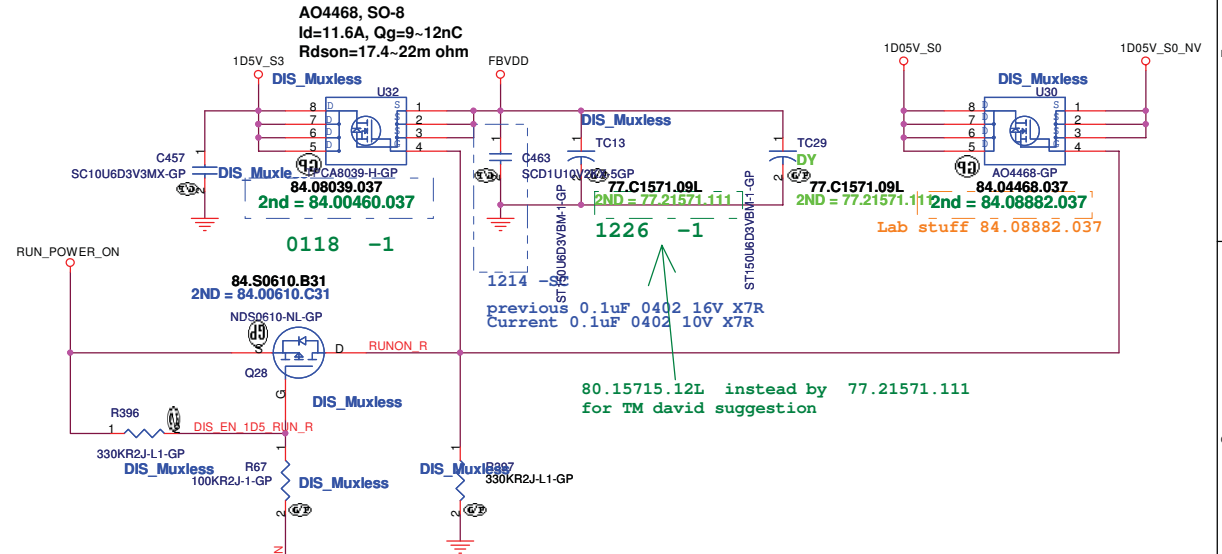
Sheet 59 of 72

+3VS to 1.8V Transfer



+1.5V to FBVDD Transfer

+1.05V to +1.05V_NV Transfer



0113 -1

16.55.62 DGPU_PWROK >>>

0113 -1

0113 -1

0113 -1

0113 -1

0113 -1

0113 -1

0113 -1

0113 -1

0113 -1

0113 -1

0113 -1

0113 -1

0113 -1

0113 -1

0113 -1

0113 -1

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0113 -1

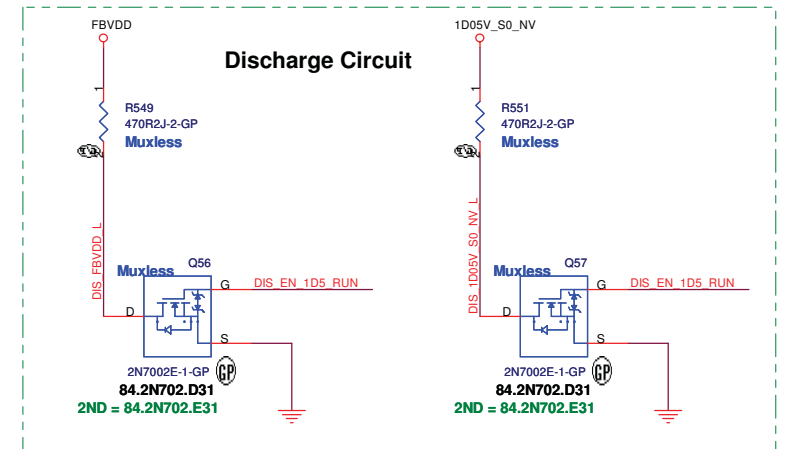
0113 -1

0113 -1

0113 -1

0113 -1

0113 -1



0113 -1

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title

NV power

Size

Document Number

HM42-CP

Rev

SC

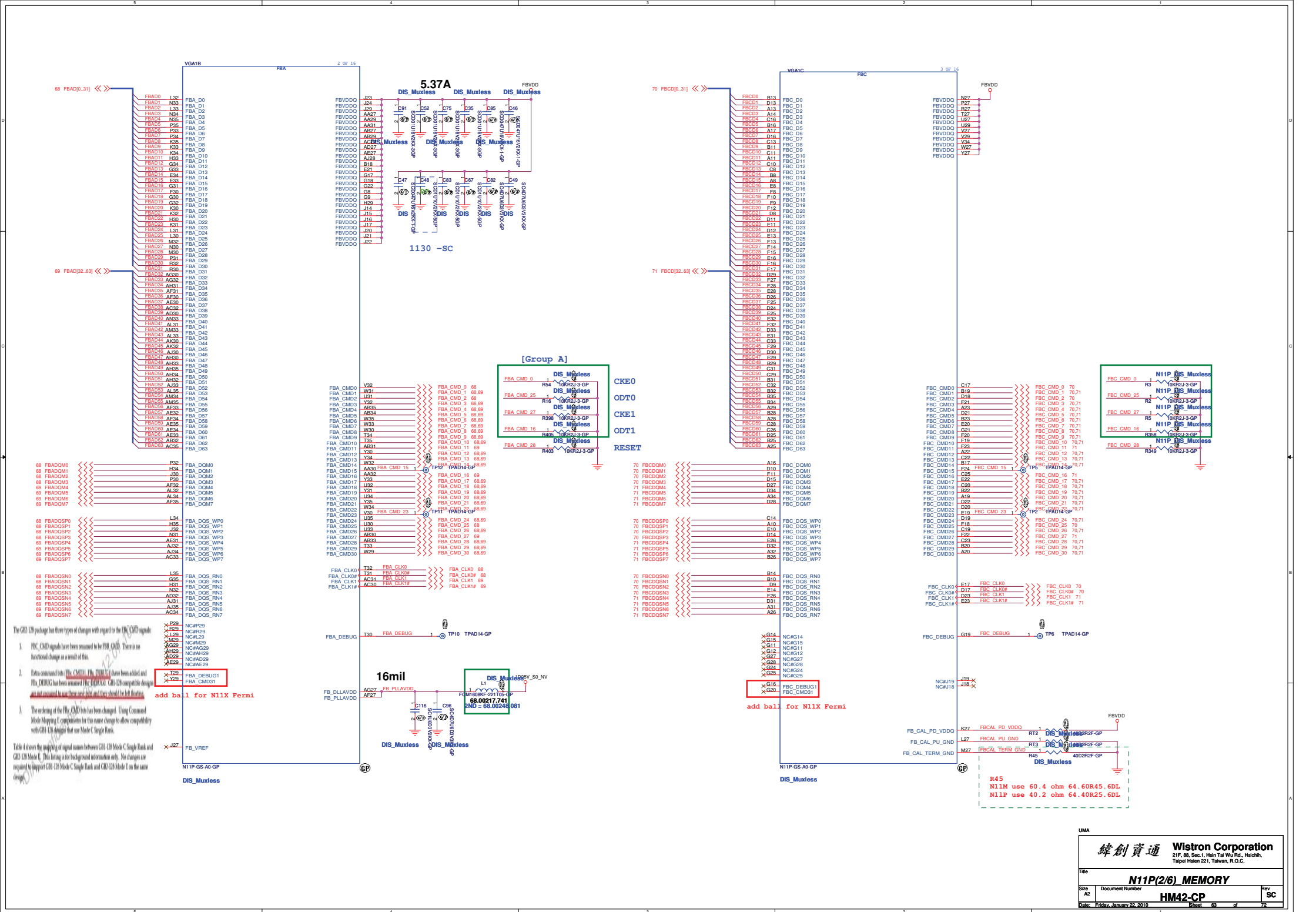
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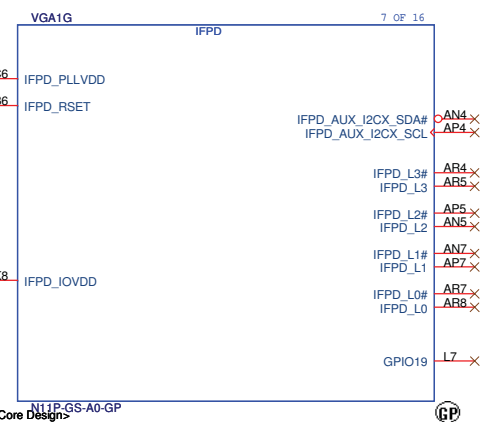
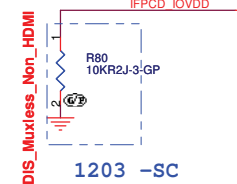
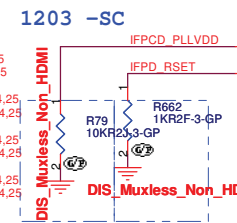
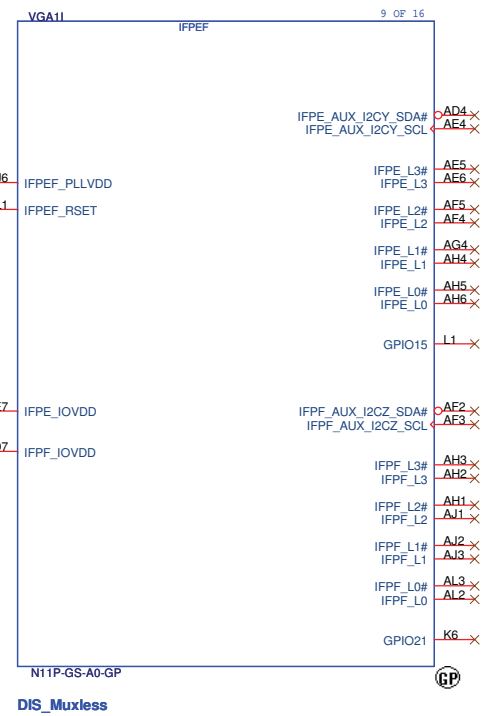
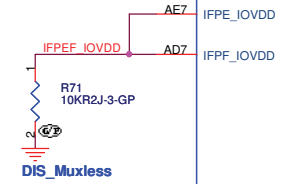
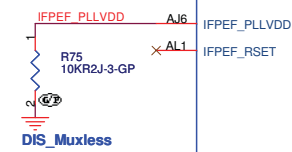
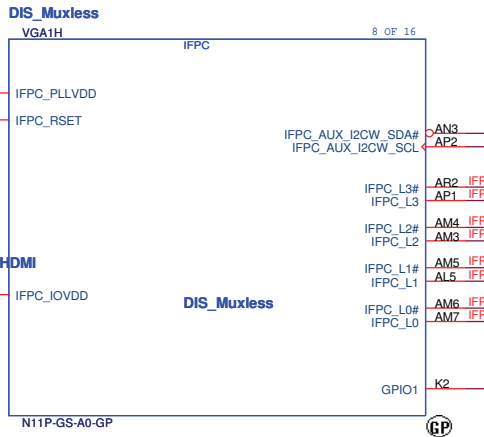
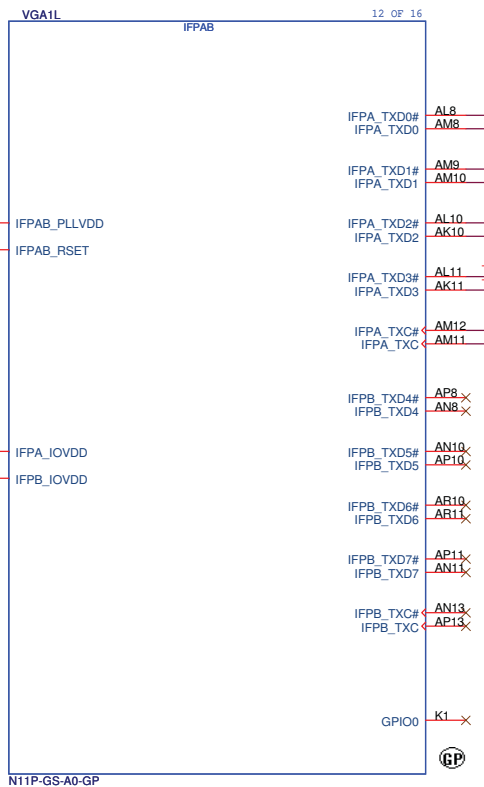
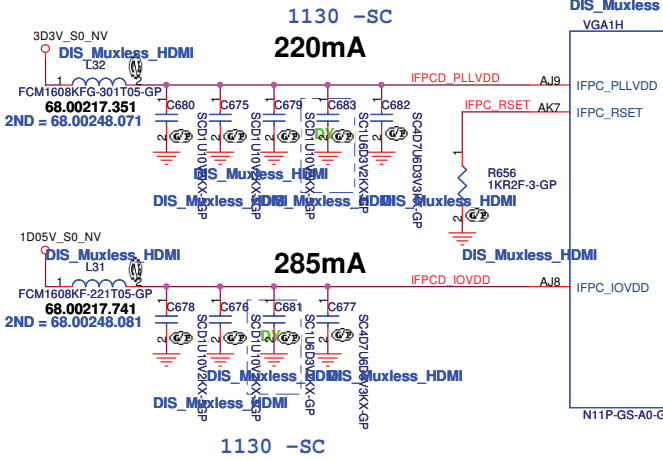
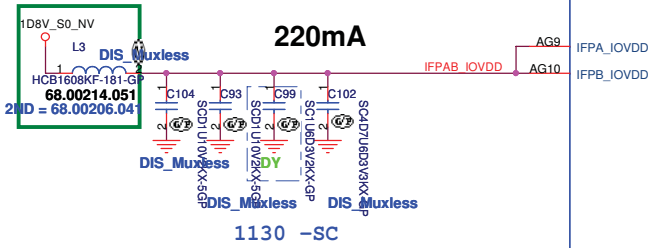
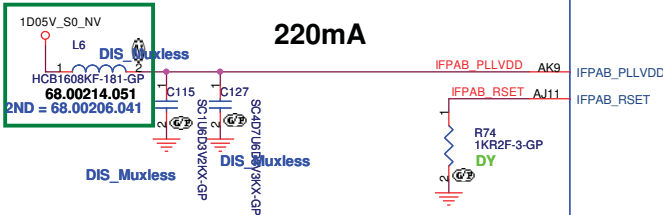
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61

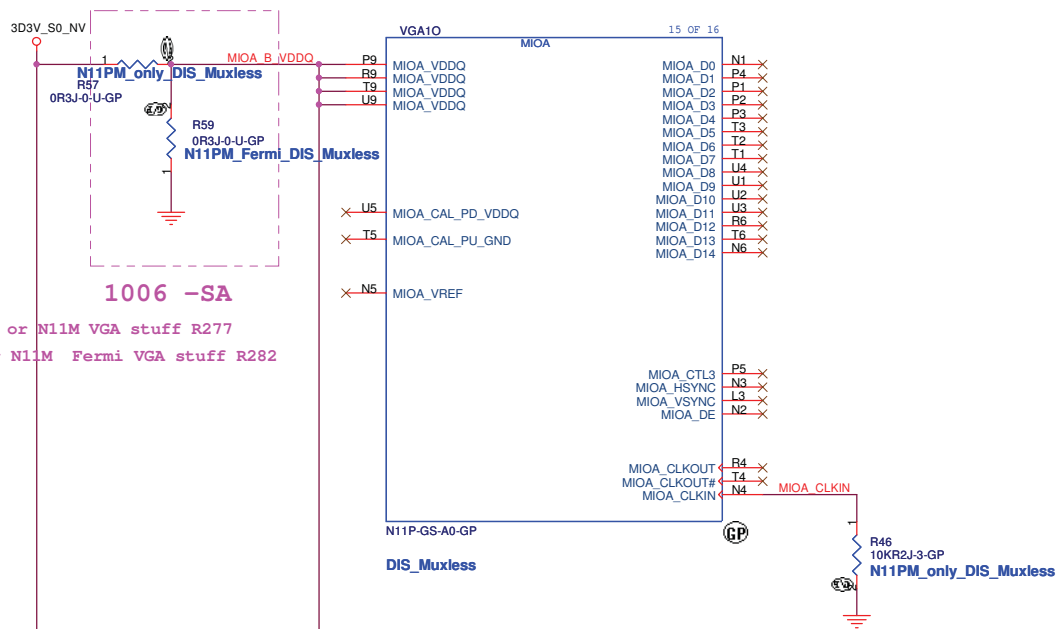
of

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120mA

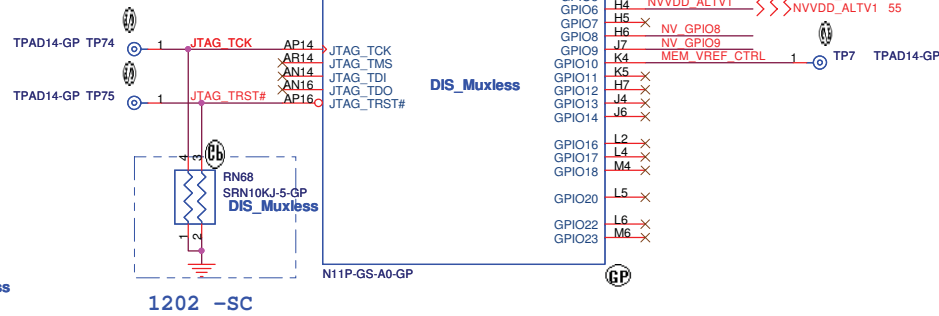
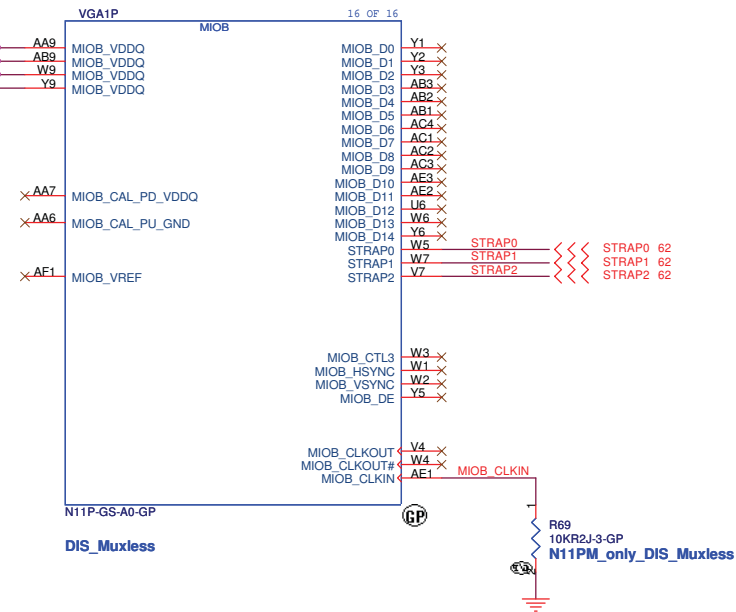


1006 -SA

N11P or N11M VGA stuff R277

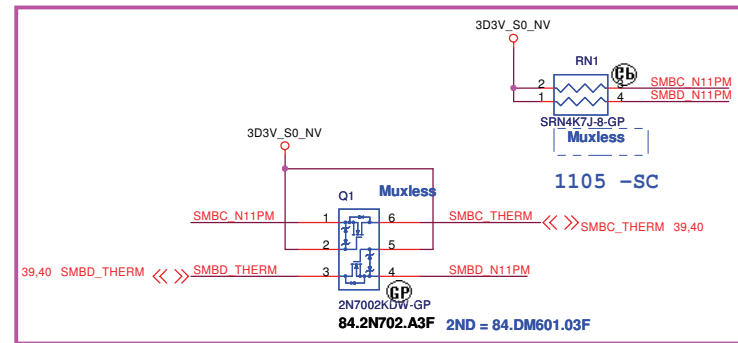
N11P or N11M Fermi VGA stuff R282

120mA

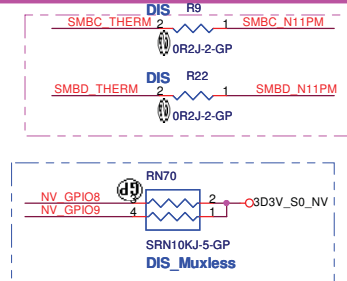


1202 -SC

HM42-CP NV Muxless SA 0916



1105 -SC



HM42-CP NV Muxless SA 0923

1202 -SC

UMA

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Title

N11P(5/6) MIO/ GPIO

Size

A3

Document Number

HM42-CP

Rev

SC

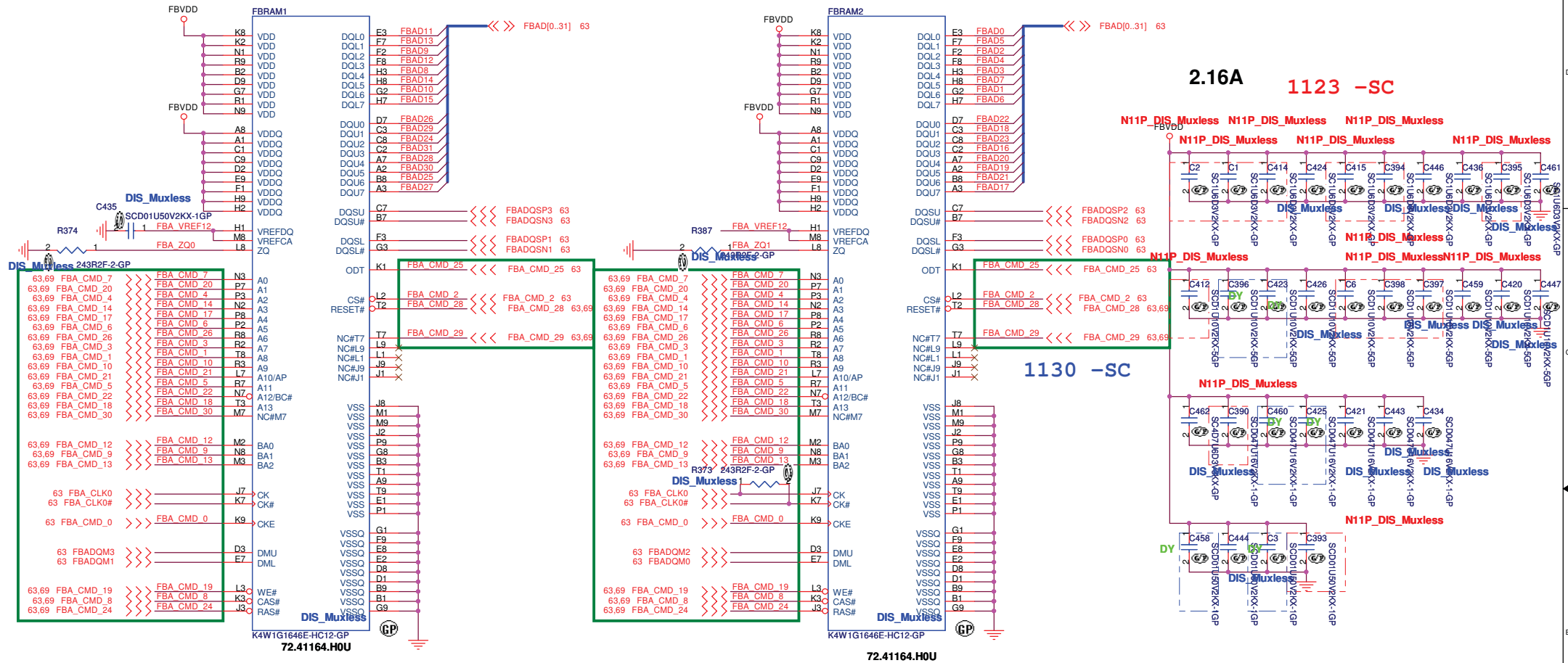
Date: Friday, January 22, 2010

Sheet 66 of 72

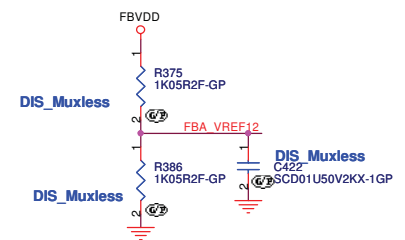


Title			
N11P(6/6) POWER			
Size A3	Document Number		Rev
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DDR3

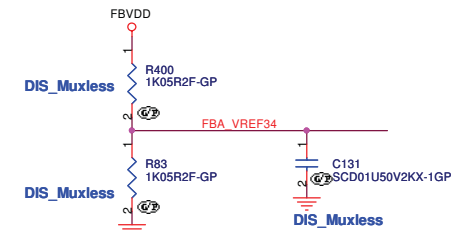
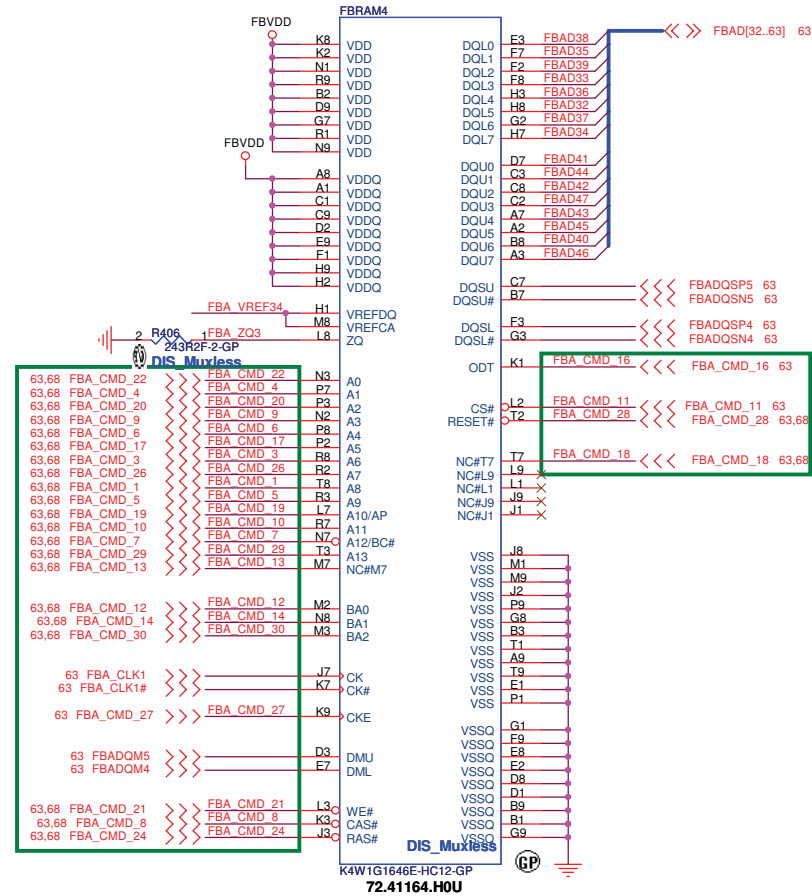
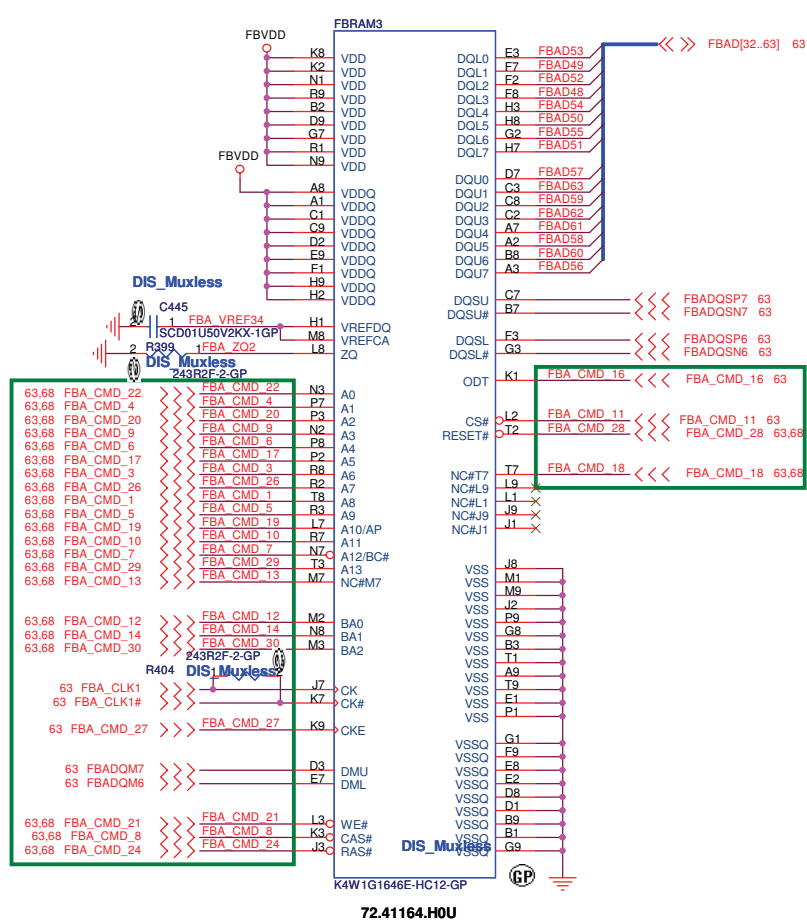


SAMSUNG: 72.41164.H0U(Use OEM PN:VR.1GB0B.006)
 HYNIX: 72.51G63.C0U(Use OEM PN: VR.1GB0G.004)



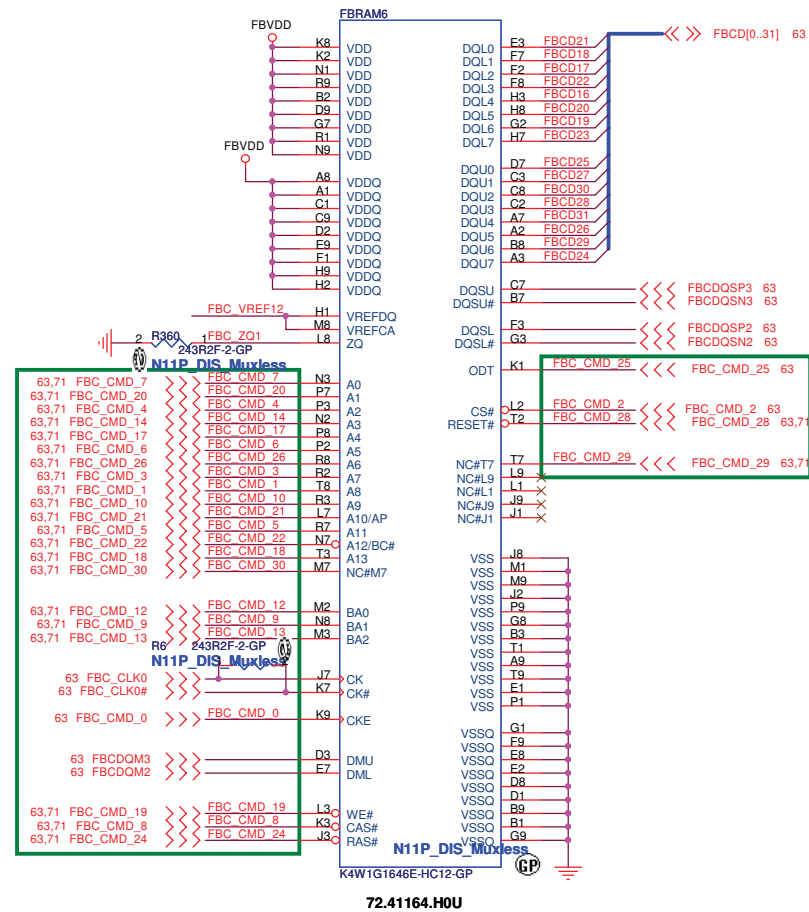
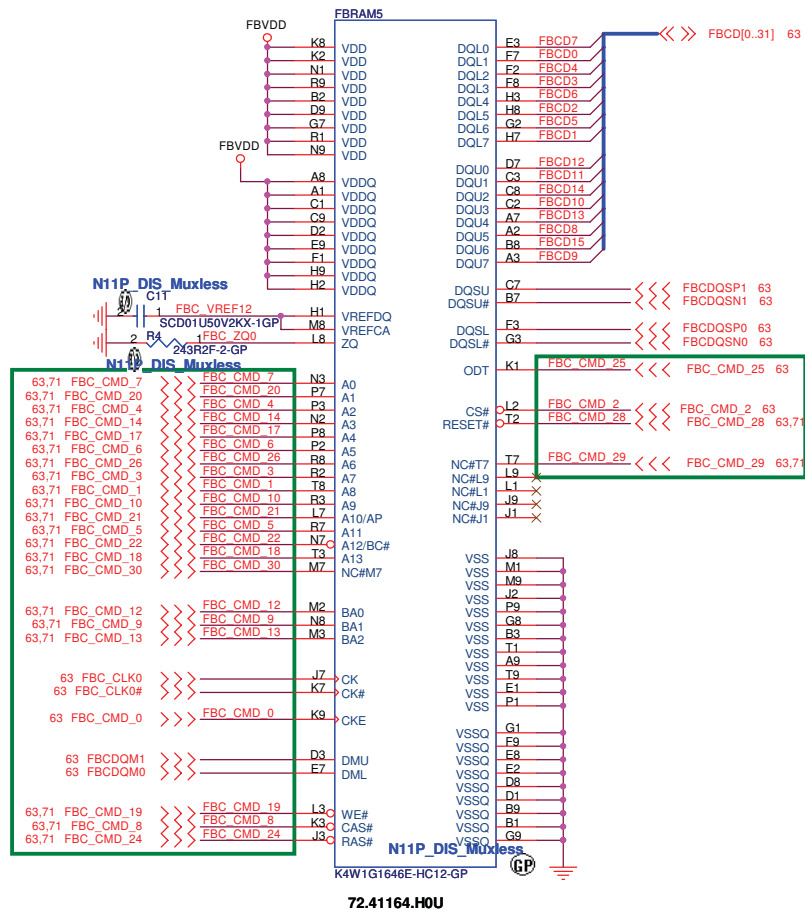
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: VRAM(1/4)	
Size: A3	Document Number: HM42-CP
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DDR3

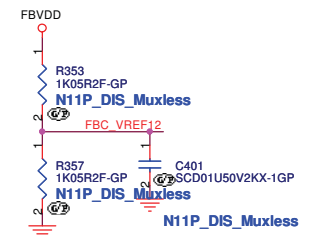


SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

DDR3



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SAMSUNG: 72.41164.H0U
HYNIX:   72.51G63.C0U
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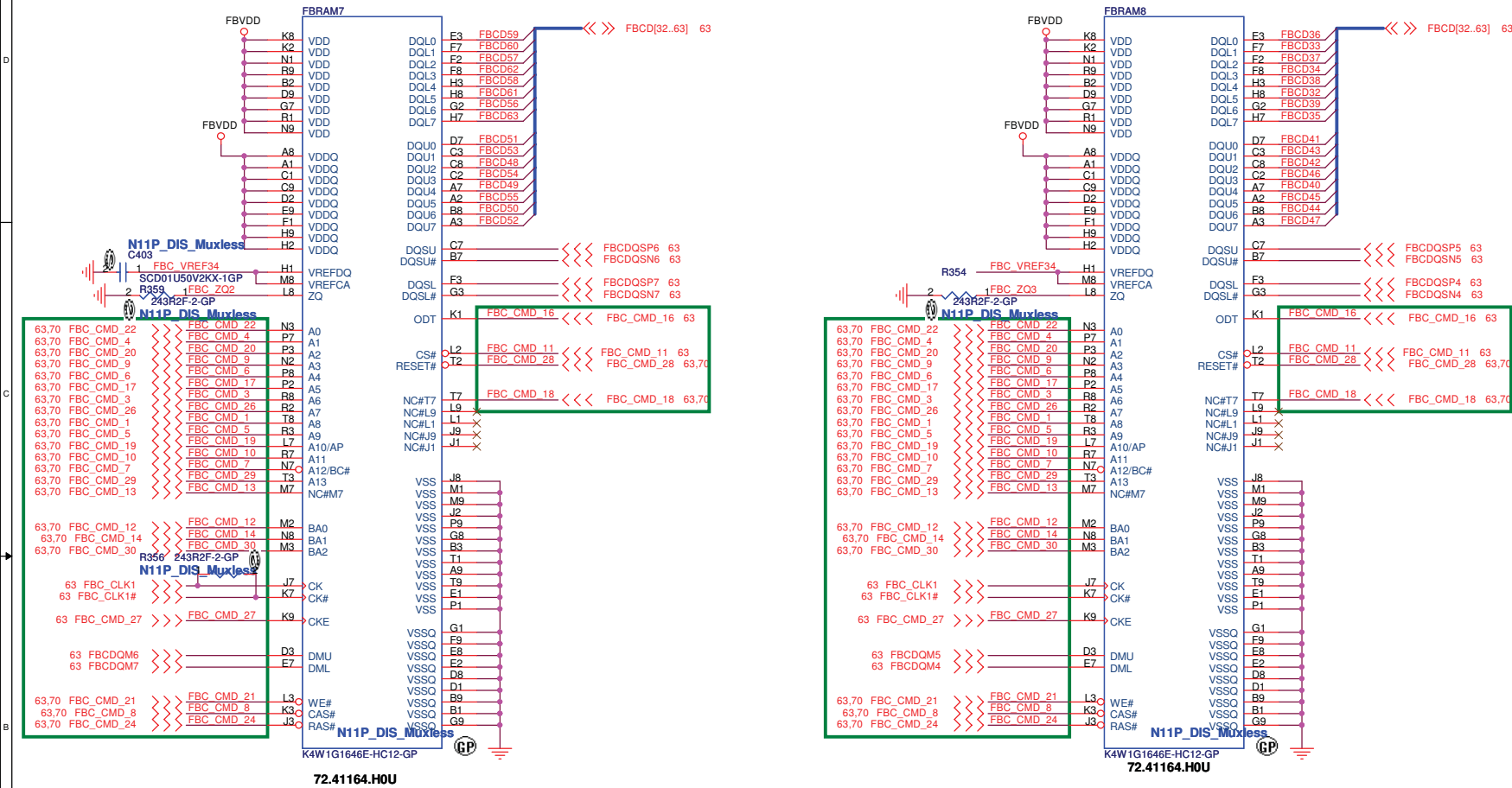


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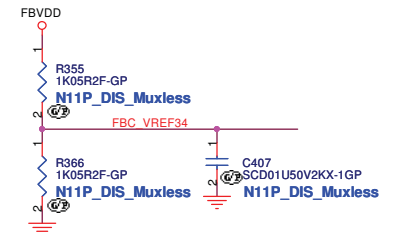
Title			
VRAM(3/4)			
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DDR3



SAMSUNG: 72.41164.H0U

HYNIX: 72.51G63.C0U



UMA

3) Samsung VRAM FBRAM1~8 PN:VR.1GB0B.006

Hynix VRAM FBRAM1~8 PN:VR.1GB0G.004

4) VGA 1 N11P-GE1 A3->71.0N11P.G0U,
N11M-GE1-B -A3 -> 71.0N11M.E0U
N11M-OP1 ->

6) VGA 1 N11P-GE1-> R53 49.9K(64.49925.6DL)
N11M-GE1 -> R53 32.4K(64.32425.6DL)

7) R26 stuff Hynix VRAM : 15K(64.15025.6DL)
Samsung VRAM : 20K(64.20025.6DL)

8) R45 stuff N11M use 60.4 ohm (64.32425.6DL)
N11P use 40.2 ohm (64.40R25.6DL)

9) Muxless SKU stuff R181 2.37K (64.23715.6DL)
UMA SKU Stuff R181 2.4K (64.24015.6DL)

10) N11M OP1 ->R392 15K(64.15025.6DL)
N11M GE1 ->R392 30K(64.30025.6DL)

Mini Card 2nd and 3rd source PN confirm

Card Reader 2nd source confrim

[ECR]

Date	released by	ECR Number
11/22	Anita	R1001240

[Old]

PCH1 PN : 71.0IBEX.A0U

[New]

PCH1 PN : 71.0HM55.00U(KI.G5501.002)

[lab -SB]

2nd -> UMA (S01G)

1st -> Diserete N11P Hynix(S02G)

1st +3rd -> Diserete N11M Hynix(S03G)

2nd +4th -> Diserete N11M Samsung(S04G)

1st -> Diserete N11P Samsung (S05G)

2nd -> N11M Hynix_support Optimus (S06G)

[Eng -SC]

2nd -> UMA Non 3G (55.4GY01.S07G)

1st -> Diserete N11P Hynix_3G(55.4GZ01.S03G)

1st +3rd -> Diserete N11M Hynix_3G(55.4GY01.S09G)

2nd +4th -> Diserete N11M Samsung_Non 3G(55.4GZ01.S02G)

1st + 5th -> Diserete N11P Samsung _3G(55.4GY01.S10G)

1st +3 rd -> UMA Non 3G Non HDMI (55.4GW01.S01G)

[PD -1]

UMA 3G (55.4GY01.M01G)

Diserete N11P Hynix_3G(55.4GY01.M02G) => 1st

Diserete N11P Hynix_Non 3G(55.4GY01.M03G) => 2nd

UMA Non 3G (55.4GY01.M04G)

Diserete N11M Hynix_3G(55.4GY01.M05G)

Diserete N11P Samsung _3G(55.4GY01.M06G) =>1 st

Diserete N11M Samsung_Non 3G(55.4GY01.M07G)

[PD action]

qual TPCN1 2nd source(20.K0296.006)

qual KB1 2nd source(20.K0382.026)

qual HDMI 2nd and 3rd

qual ODD1 3rd source(62.10065.E01)

qual PWRCN1 2nd and 3rd

qual RTC1 4th source

qual BT1 2nd and 3 source

qual U51 and U15 2nd source

qual TC13 2nd source(77.21571.111)

qual U32 2nd source

Qual HS1,HS2 2nd: 34.4B417.401

UMA

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Size

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